CMOS Analog Spectrum Processing Techniques for Cognitive Radio Applications

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CMOS Analog Spectrum Processing

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LIST OF ABBREVIATIONS

8-VSB	8-level vestigial sideband modulation
AAC	Analog auto-correlation
AAF	anti-aliasing filter
ADC	analog-to-digital converter
ATSC	American television standard committee
AWGN	additive white Gaussian noise
BER	bit error rate
CR	cognitive radio
CW	continuous wave
D/U	desired-to-undesired
DAC	digital-to-analog converter
DSM	delta-sigma ($\Delta\Sigma$) modulator
DTV	digital television
DVB	digital video broadcasting
DVB-T	digital video broadcasting – terrestrial
DWG	digital window generator
EVM	error vector magnitude
FFT	fast Fourier transform
GUI	graphic user interface
IC	integrated circuit
LNA	low-noise amplifier

LPF	low-pass filter
MAC	media access control
MASH	multi-stage noise shaping
MIMO	multiple input, multiple output
MRSS	multi-resolution spectrum sensing
NF	noise figure
OFDM	orthogonal frequency-division multiplexing
OFDMA	orthogonal frequency-division multiple access
P_{1dB}	1dB gain-compression point
PA	power amplifier
PC	personal computer
PDF	power density function
PHY	physical layer
PLL	phase locked loop
PN	pseudo-random noise
PVT	process, supply voltage, and operating temperature
PWM	pulse-width modulation
RAM	random access memory
SAW	surface acoustic wave
SNR	signal-to-noise ratio
SRAM	static random access memory
UHF	ultra high frequency
UWB	ultra wideband

VCO	voltage-controlled oscillator
VGA	variable-gain amplifier
WiMax	worldwide interoperability for microwave access
WLAN	wireless local area network
WRAN	wireless regional area network

SUMMARY

The objective of the research is to develop analog spectrum processing techniques for cognitive radio (CR) applications in CMOS technology.

CR systems aim to use the unoccupied spectrum allocations without any license when the primary users are not present. Therefore, the successful deployment of CR systems relies on their ability to accurately sense the spectrum usage status over a wide frequency range serving various wireless communication standards. Meanwhile, to maximize the utilization of the available spectrum segments, the bandwidth of the signal has to be highly flexible, so that even a small fraction of spectrum resources can be fully utilized by CR users. One of the key enabling technologies of variable bandwidth communication is a tunable baseband filter.

In this research, a reconfigurable CR testbed system is presented as groundwork for the researches related with CR systems. With the feasibility study on the multi-resolution spectrum sensing (MRSS) functionality, a method for determining sensing threshold for MRSS functionality is presented, and a fully integrated MRSS receiver in CMOS technology is demonstrated. On the other hand, a reconfigurable CMOS analog baseband filter which can change its bandwidth, type and order with high resolution for CR applications is presented. In sum, an analog spectrum sensing method as well as a highly flexible analog baseband filter architecture is established and implemented in CMOS technology. Both designs are targeting the utilization of the analog signal processing capability with the aid of the digital circuits.

CHAPTER 1

INTRODUCTION

1.1. Technology Trends

As the use of the electromagnetic spectrum for the wireless communication increases, the danger of interference between users has made governments impose regulations over its usage. With the tremendous growth of wireless applications, many spectrum segments have been allocated to licensed spectrum users. Figure 1 shows the frequency allocation chart from 30 MHz to 3 GHz as of October 2003 in the United States [1]. The ever-growing demand for higher user data rates has driven the wireless communication industry to implement more efficient modulation techniques or sophisticated coding schemes in its limited spectrum allocations. These licensees have the privileged rights to use this authorized spectrum for commercial or public use.

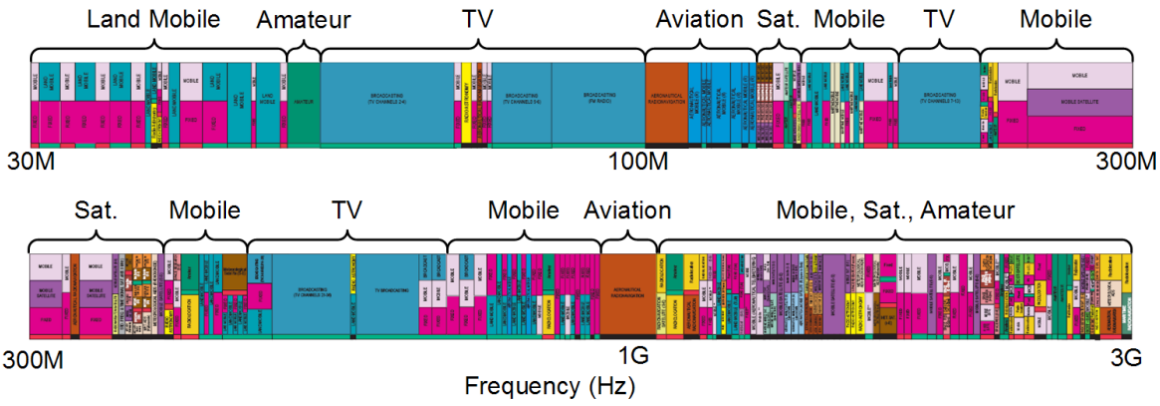


Figure 1. United States frequency allocation chart as of October 2003.

When the licensed spectrum band is carefully observed, however, some spectrum segments are found to be much less than fully utilized, depending on time and location [2], [3]. Figure 2 shows the spectrum utilization of less than 2 GHz of a spectrum segment in New York city during 24 hours on August 31, 2004 [3]. The red dot represents that the spectrum is occupied for that specific time. From this figure, it is clear that not all the spectrum segment is occupied all the time. Only a small portion of the spectrum is heavily used, making the average usage about 13%. Therefore, researchers in wireless technology have been demanded to create a new wireless communication system to use the spectrum more efficiently than in the past [2].

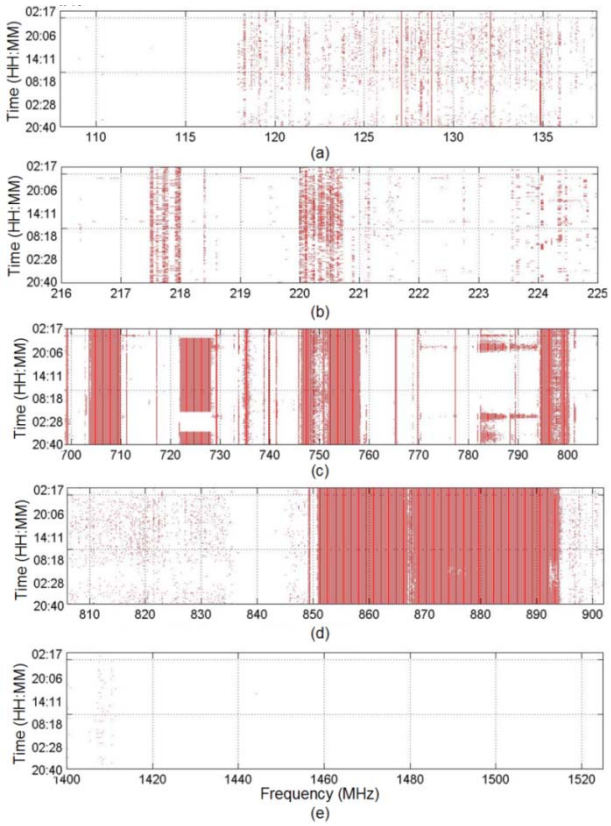


Figure 2. Spectrum utilization in New York City during 24 hours on August 31, 2004 in (a) aviation band, (b) maritime mobile and amateur band, (c) ultra high frequency (UHF) TV band, (d) handset and base station, and (e) satellite and telemetry band.

Recently, cognitive radio (CR) technology has been proposed as a promising solution to improve the efficiency of spectrum usage by adopting a dynamic spectrum resource management concept [4], [5]. CR systems aim to use the unoccupied spectrum allocations without additional license when the primary (i.e., licensed) users are not present. Therefore, a CR system should have flexible transceiver architecture to adapt itself for the varying environment, covering multiple communication standards over a wide frequency range.

There are distinctive movements in standardization groups to adopt the CR concept. IEEE 802.22 wireless regional area network (WRAN) is a first application with the concept of CR in the U.S. digital television (DTV) band, targeting to provide broadband access in rural areas [6]. The target service range is 33 km with the frequency range from 54 MHz to 862 MHz by using orthogonal frequency-division multiple access (OFDMA) scheme. On the other hand, on November 2008, Federal communications commission (FCC) approved white space for the unlicensed use of U.S. DTV bands [7]. It specifies two kinds of devices to be allowed in the white space, a fixed device and a personal portable device, opening a way to use CR technology in a mobile device.

For the success of CR systems, various spectrum processing techniques should be implemented to sense and select the desired spectrum resources. To maximize the throughput of CR systems, those spectrum processing techniques should be highly flexible and reconfigurable to be adaptive, depending on the availability of spectrum resources.

1.2. Motivation for Dissertation

Spectrum processing techniques for CR applications can be categorized into spectrum sensing technique and spectrum filtering technique.

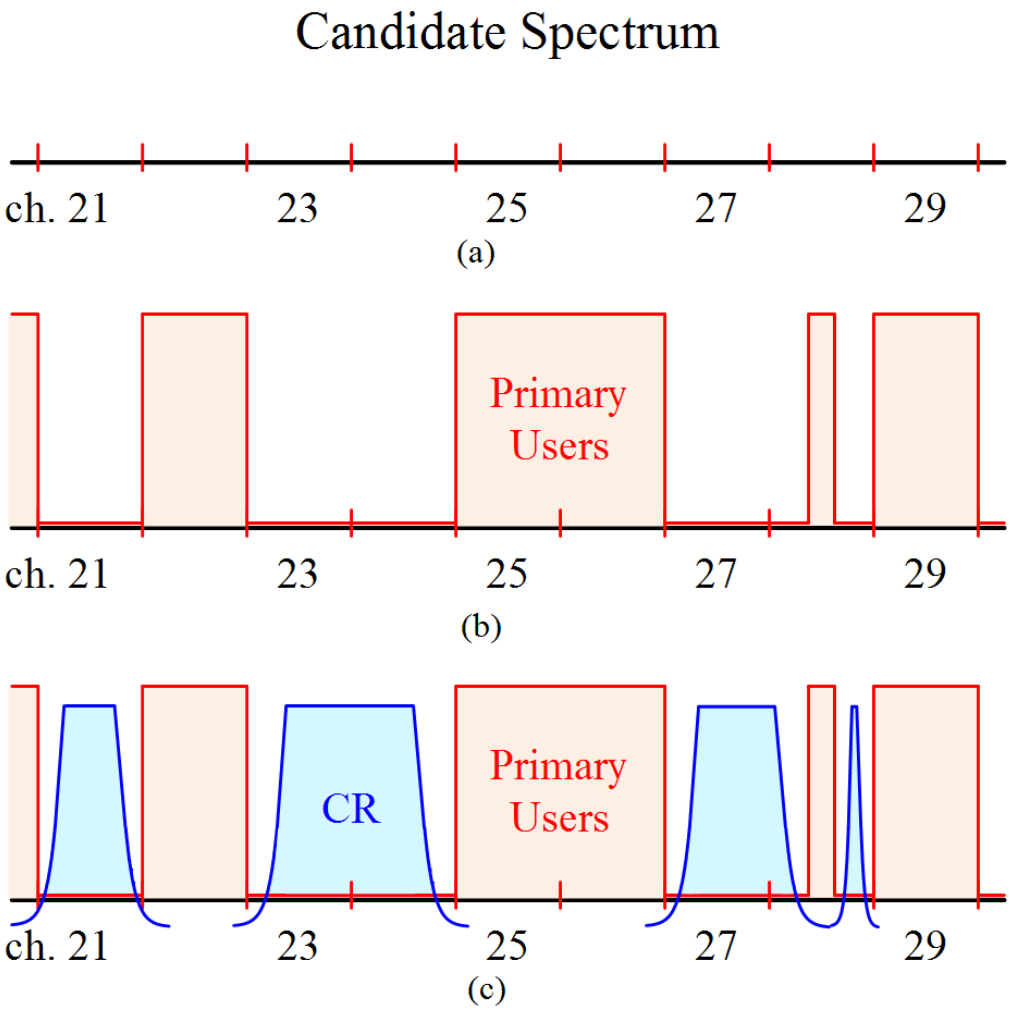


Figure 3. An example of CR operation, showing (a) a candidate spectrum frequency band, (b) spectrum segments occupied by multiple primary users, and (c) CR users occupying vacant spectrum segements.

Figure 3 shows an example of CR operation. Let's assume that there is a candidate spectrum band from DTV channel 21 to channel 29 where CR operation is allowed, as shown in Figure 3(a). Figure 3(b) shows a possible occupation of that spectrum band by primary users. In order not to violate the licensee's right to exclusively use the allocated spectrum segments, the CR system should avoid using any spectrum segments already occupied by primary users. Moreover, even though CR users have been using the vacant

spectrum, CR users should stop their communication whenever any primary user wants to use that band in order not to interfere with primary users. If those protections are not provided, the CR system would not be allowed to utilize the vacant spectrum resources. Therefore, the successful deployment of the CR system relies on its ability to accurately sense the spectrum usage status over a wide frequency range serving various wireless communication standards. Meanwhile, spectrum filtering functionality is essential to increase the throughput of CR systems. Because there is no guarantee on the availability of spectrum segments, even a small fraction of the spectrum should be fully utilized through channel bonding or channel splitting, as shown in Figure 3(c). The danger of interference between CR users and primary users should be also carefully controlled. One of the key enabling technologies of variable bandwidth communication is a tunable baseband filter that can change its bandwidth, type, and order as needed.

The most crucial requirements for spectrum sensing are sensing sensitivity and sensing time to protect incumbent users and to improve data throughput. Lower sensitivity prevents a CR system from being adopted because of the danger of infringing upon incumbent users. Longer sensing time will reduce throughput for the CR system and create longer possible interference to primary users. In addition, low power consumption and simple implementation are desirable features from a CR system commercialization viewpoint [6].

For successful reception of the signal with the presence of the interferers, those undesirable signals should be filtered out before digitized by an analog-to-digital converter (ADC) for further processing in a digital domain. On the other hand, the transmitted signal bandwidth should be confined to a specified spectrum mask in order to not interfere with other communication systems. With the demand for agile adaptation to the communication

environment, CR systems should support a wide tuning range on their spectrum filtering and selectivity.

The objective of the research in this dissertation is to develop analog spectrum processing techniques for CR applications in CMOS technology. In this research, an analog spectrum sensing method as well as a highly flexible analog baseband filter architecture is established and implemented in CMOS technology. Both designs are targeting the utilization of the analog signal processing capability with the aid of the digital circuits. The contributions of this research will be as follows:

1. A reconfigurable CR testbed system will be established as groundwork for the researches related with CR systems.
2. The feasibility of the multi-resolution spectrum sensing (MRSS) functionality will be investigated.
3. A method for determining sensing threshold for MRSS functionality will be discussed.
4. A fully integrated MRSS receiver in CMOS technology will be demonstrated.
5. A reconfigurable CMOS analog baseband filter which can change its bandwidth, type, and order with high resolution for CR applications will be presented.

1.3. Organization of Dissertation

This dissertation consists of seven chapters.

Chapter 2 presents a reconfigurable CR testbed system for easy verification of the new concepts and the test of the fabricated circuits. For the evaluation of this CR testbed system,

the CR system concept demonstration and the interference analysis for ultra wideband (UWB) coexistence with the worldwide interoperability for microwave access (WiMax) system are shown.

Chapter 3 explains on spectrum sensing technique. The conventional spectrum sensing methods are reviewed, and the proposed feature detection and energy detection methods are presented. Both methods aim to relax the requirements of the analog-to-digital converter (ADC) by performing most of computations in the analog domain. The proposed feature detection method is called as analog auto-correlation (AAC), and the proposed energy detection method is named as multi-resolution spectrum sensing (MRSS).

Chapter 4 discusses on the sensing threshold level determination method for MRSS technique. After introducing the spectrum sensing scenario, the statistical distribution of MRSS on the white Gaussian noise is investigated. From this model, the minimum sensing threshold level can be derived given the probability of false alarm and the receiver specifications. With the threshold level, the probability of misdetection is derived and compared with simulation results. Also, the effect of phase noise on the detection is investigated.

Chapter 5 presents the design of a fully integrated MRSS receiver in 0.18 μm CMOS technology. The overall architecture and the key building blocks such as the digital window generator (DWG) and the analog correlator are investigated. Measurements using a CR testbed system show that MRSS receiver can work like a simple spectrum analyzer embedded into a receiver.

Chapter 6 introduces the design of a reconfigurable CMOS analog baseband filter which can change its bandwidth, type, and order with high resolution for CR applications. A

highly flexible and reconfigurable analog baseband filter is an essential building block for the filtering and the selection of the desired spectrum segment. A baseband filter which can change its bandwidth, frequency response, and order of a filter with simple architecture and low power consumption is desired for the adoption in a CR system. By using $\Delta\Sigma$ modulation as a way of having fractional control resolution, the proposed filter can have fine resolution on its configurability.

Chapter 7 concludes this dissertation with a discussion on the future works.

CHAPTER 2

COGNITIVE RADIO TESTBED SYSTEM

2.1. Motivation for the Cross-layer Cognitive Radio Testbed

To provide a versatile environment for developing various CR technologies, a reconfigurable testbed system is required [8]. This testbed should be flexible enough to incorporate the developed system concept, signal processing techniques and the implemented hardware into the existing testbed. Moreover, a fully automated environment is preferred in order to facilitate the evaluation process. The incorporation of various standard formats on signal generation and analysis allows for comparing the performance with existing solutions.

2.2. CR Testbed Overview

As the CR concept is incorporated into emerging wireless standards, a reconfigurable testbed system is essential in validating proposed signal processing techniques and their hardware implementations. To support thorough testing of its own CR system and integrated circuit (IC) designs, a multi-standard, fully software-driven testbed system has been developed. The purpose of the CR testbed is (1) to demonstrate the CR system concept, (2) to evaluate various spectrum sensing technologies, (3) to develop RF/analog circuits and systems technology, (4) to evaluate the physical layer (PHY), media access control (MAC), and network technologies, and (5) to explore the co-existence scenarios for heterogeneous communication systems.

This testbed system has a capability of instant testing and evaluation of the algorithm levels of the communication system and of the RF/analog ICs. Once a core IC or new algorithm has been developed, it will be incorporated into the CR testbed to see how much impact it has on the real system. Figure 4 is a photograph of cross-layer CR testbed demonstrating the concept of CR.

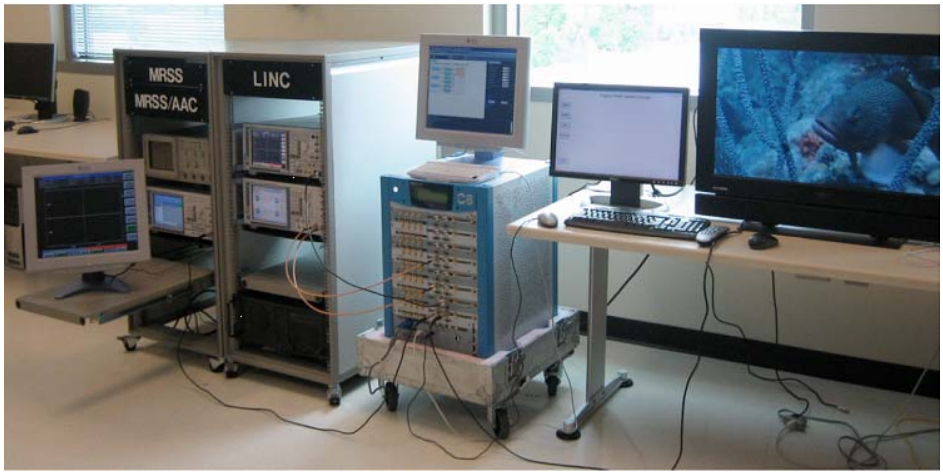


Figure 4. A photograph of cross-layer cognitive radio testbed.

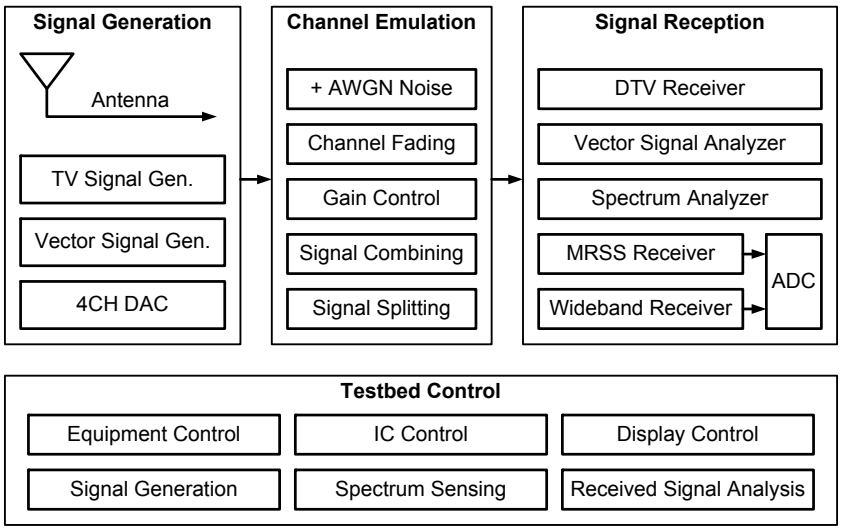


Figure 5. Cross-layer cognitive radio testbed configuration.

Figure 5 illustrates the configuration capabilities of the testbed system. The testbed is composed of signal generation, channel emulation, signal reception, and testbed control parts.

Signal generation makes various types of signals either by capturing a RF signal from an antenna or by generating signals from equipment such as a TV signal generator, a vector signal generator, and a four-channel digital-to-analog converter (DAC). Equipment provides a variety of built-in standard wireless signals such as IEEE 802.16, IEEE 802.11a/b/g, 3G-wireless, cellular, American television standard committee (ATSC), digital video broadcasting (DVB), etc. If a custom-generated baseband signal within 100 MHz of the bandwidth is available, those signals can be downloaded to a vector signal generator to modulate and upconvert them to an arbitrary carrier frequency with the given sampling frequency. So, virtually any kind of signal can be employed in this testbed.

Channel emulation manipulates the generated signals to reflect the non-idealities of a real environment. This can be done by adding white Gaussian noise and applying channel fading and shading models. Gain control and signal combining or splitting can also be done in this stage. Moreover, up to a 4×4 multiple input, multiple output (MIMO) environment can be emulated.

Signal reception analyzes the quality of signals in various ways, depending on the type of a signal we want to evaluate. For a DTV signal, a DTV receiver can display the live picture on a wide flat-panel screen. A vector signal analyzer can show the constellation or error vector magnitude (EVM) and extract raw data for further signal processing. A spectrum analyzer displays the spectrum usage in real time. With a wideband receiver, the input signal can be digitized by an analog-to-digital converter (ADC) for post processing.

The custom-designed ICs can also be placed in this part, enabling the evaluation of hardware performance.

Table 1. Specifications of cross-layer cognitive radio testbed building blocks.

Name	Specification
SFU	TV signal generator RF output – 100 kHz ~ 3 GHz Standard – ATSC, DVB-T/H/C/S, DMB-T, DIRECTV, T-DMB/DAB, analog TV, arbitrary signal, etc Test stream generator Noise – additive white Gaussian noise (AWGN), phase noise, impulsive noise Fading – static path, pure Doppler, Rayleigh, rice, const. phase
SMU 200A	Vector signal generator Dual RF path – A (100 kHz ~ 3 GHz), B (100 kHz ~ 3 GHz) I/Q baseband modulation bandwidth – 56 MHz
DAC	PCI-interface 4 channel / 12-bit resolution Max. 300 MSamples/sec
C8	Channel emulator Fading, AWGN noise modeling Signal combine/divide, gain control 4×4 MIMO
FSQ 40	Vector Signal Analyzer, Spectrum Analyzer RF input – 20 Hz ~ 40 GHz Standard – GSM/EDGE, CDMA2K, Bluetooth, WLAN, WiMax, etc
MRSS Receiver	UHF receiver with multi-resolution spectrum sensing functionality Custom designed chip: TSMC 0.18μm CMOS technology Receiver mode / MRSS mode Digitally controllable through the serial bus interface
Wideband Receiver	RF input – 50 ~ 878 MHz IF out at 44 MHz / 6-MHz surface acoustic wave (SAW) filter can be bypassed Noise figure (NF): 8 dB / RF VGA gain control: -12 ~ 38 dB
ADC	PCI-interface Dual channel / 12-bit resolution Max. 400 MSamples/sec Input dynamic range : 100 mV ~ 5 V
H/W Interface	Ethernet USB-to-IEEE488.2 Interface Converter Parallel port

The testbed is fully automated by using a MATLAB™-based customized software program that provides equipment control, custom-designed IC control, graphic user interface (GUI) control, signal generation, spectrum sensing algorithm, and received signal analysis. All the equipment and components are connected using Ethernet, IEEE 488.2 interface or parallel port, or are installed in a personal computer (PC) and controlled from a GUI.

2.3. Testbed Evaluation Scenarios

2.3.1. CR System Concept Demonstration

To show the versatility of this cross-layer CR testbed, a CR system concept demonstration has been performed. The purpose of this demonstration is to visually show the concept of CR so everyone can understand the purpose and the requirement of CR.

Figure 6 shows the configuration of CR testbed for this demonstration scenario.

The input signal for this demonstration is a live air signal captured by an indoor antenna from 595 MHz to 647 MHz. In this band, analog TV signals and digital TV signals are present together. If the demonstration is performed where antenna signal reception is impossible, a TV signal generator can be used to generate various TV signals. A vector signal generator is used to emulate CR signals using WiMax standard signals at the carrier frequency we want. Channel emulation is used to control the signal power and redistribute signals to various destinations. A DTV receiver tries to show the live picture centered at 623 MHz, and a vector signal analyzer tries to evaluate CR signals. A wideband receiver followed by an ADC sends the digitized signal to a PC to execute the spectrum sensing algorithm and show the spectrum usage states.

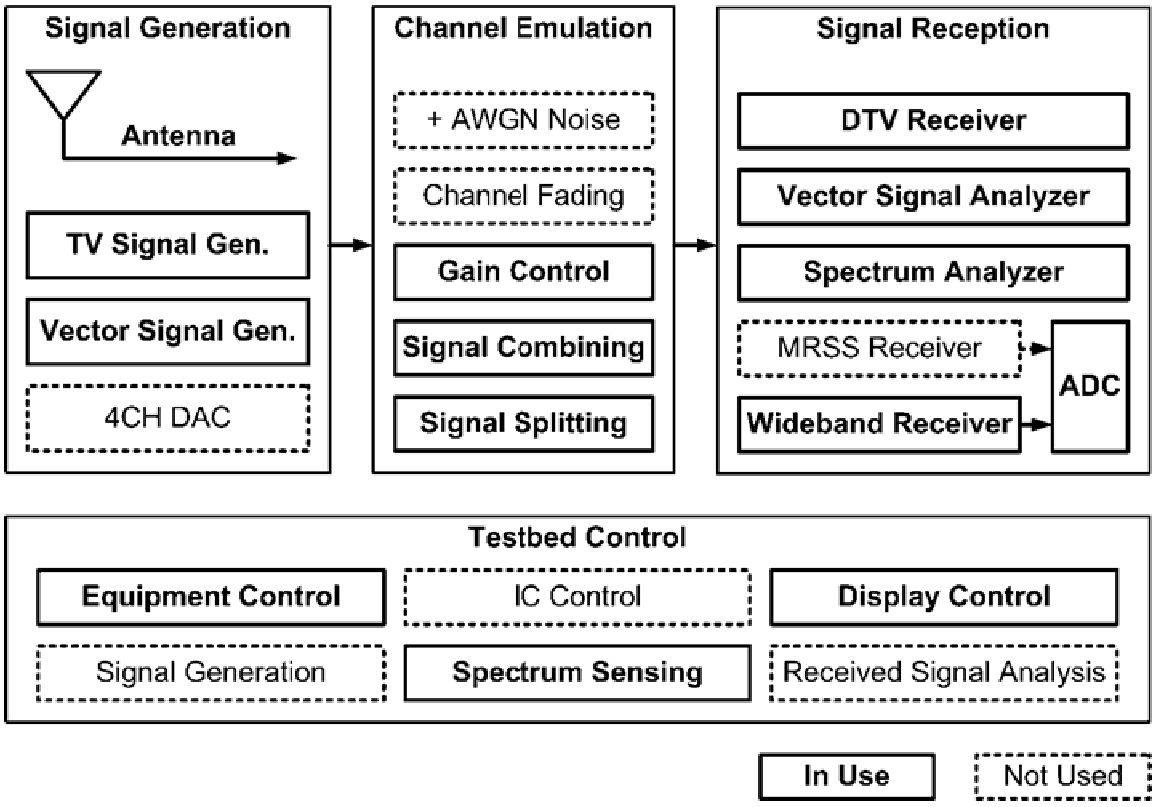
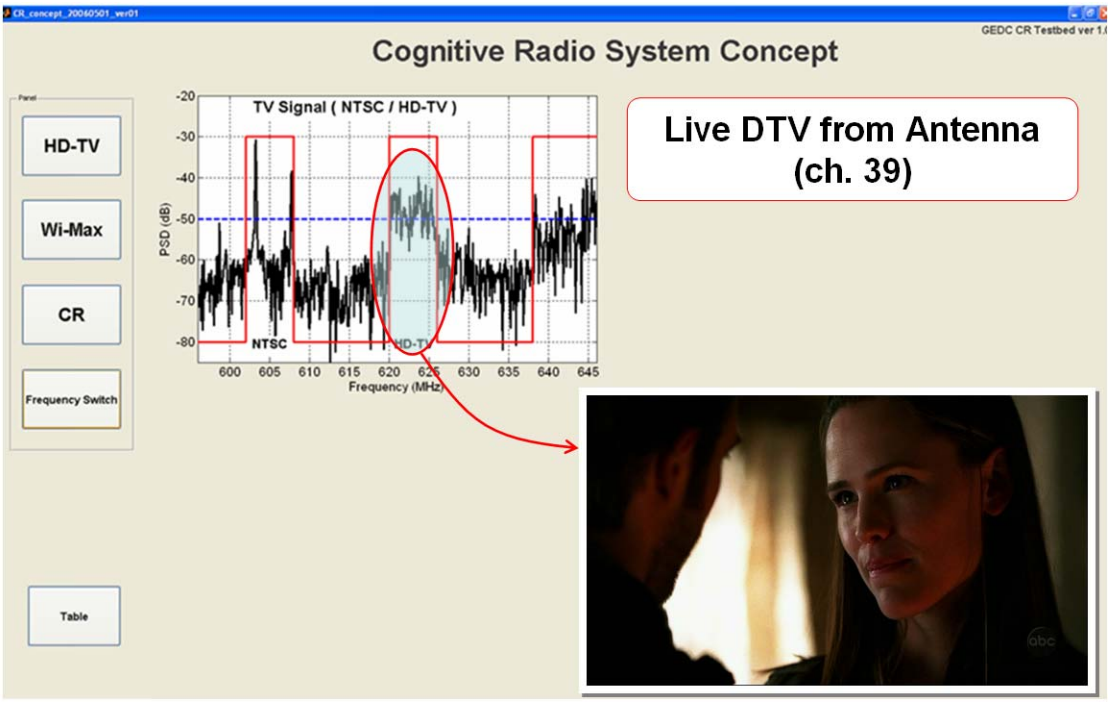


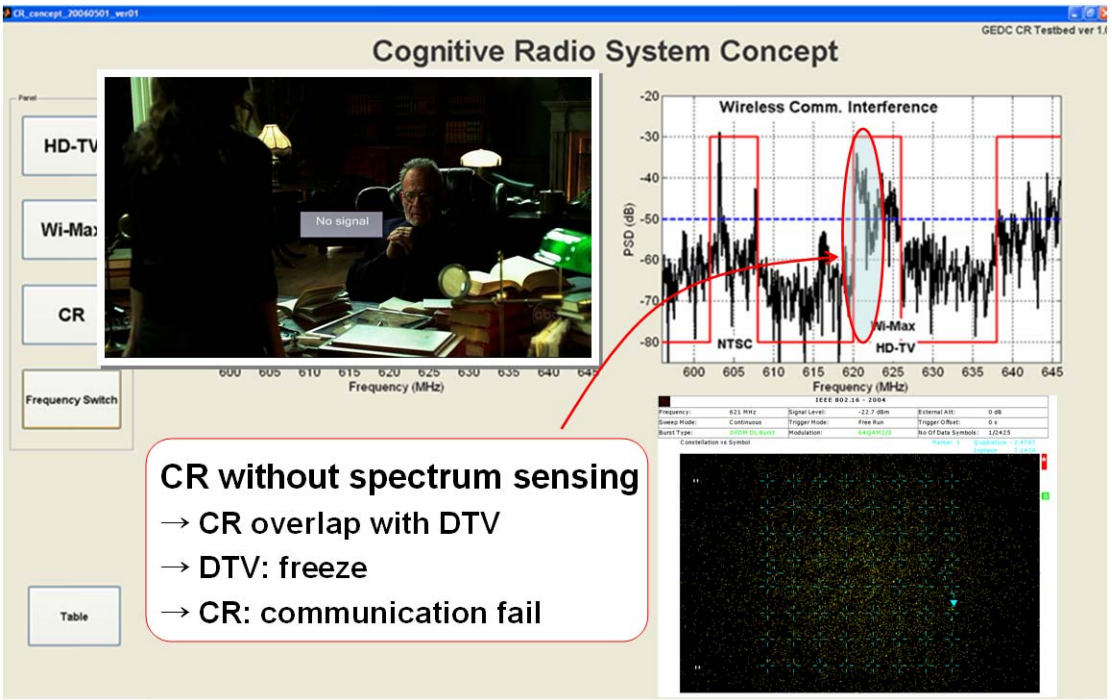
Figure 6. CR testbed configuration for a cognitive radio system concept demonstration.

Figure 7 shows a snapshot of a GUI at each stage of the demonstration. The demonstration scenario is as follows:

(a) TV broadcasters are the primary users in the UHF band. This shows when no CR users are present, so no interference is present for TV. At this time, DTV is live-streamed to a TV screen. The spectrum statues is the result of the spectrum sensing algorithm run on a PC, showing complete spectrum distribution, detection threshold, and channel occupancy.

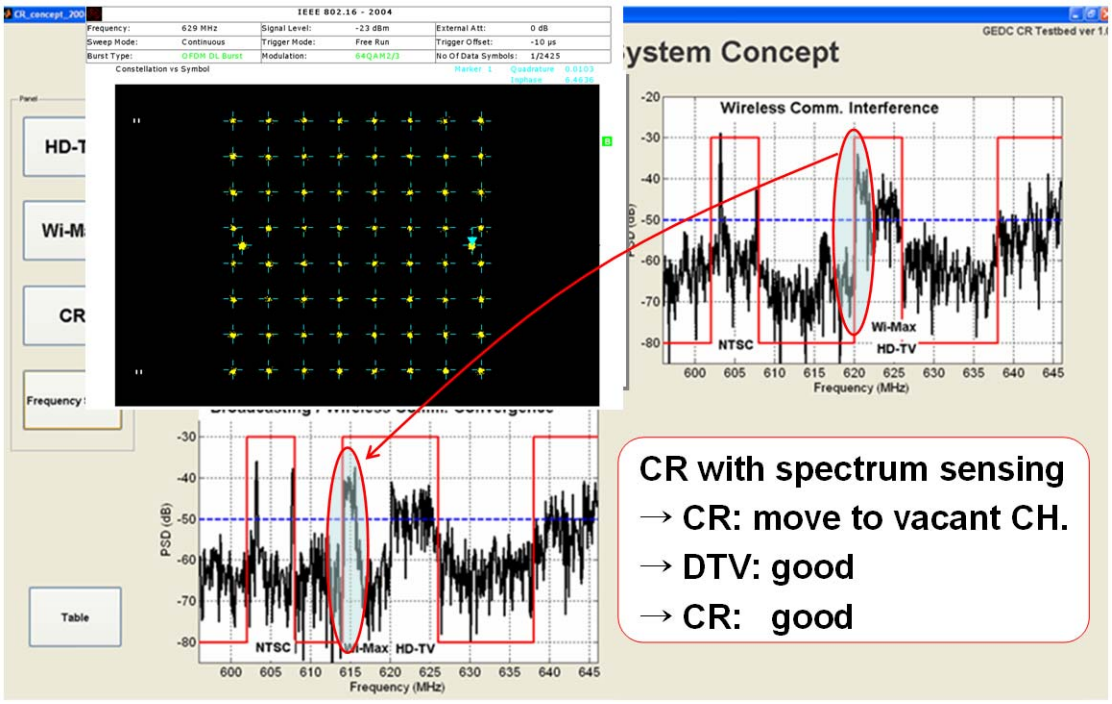


(a)

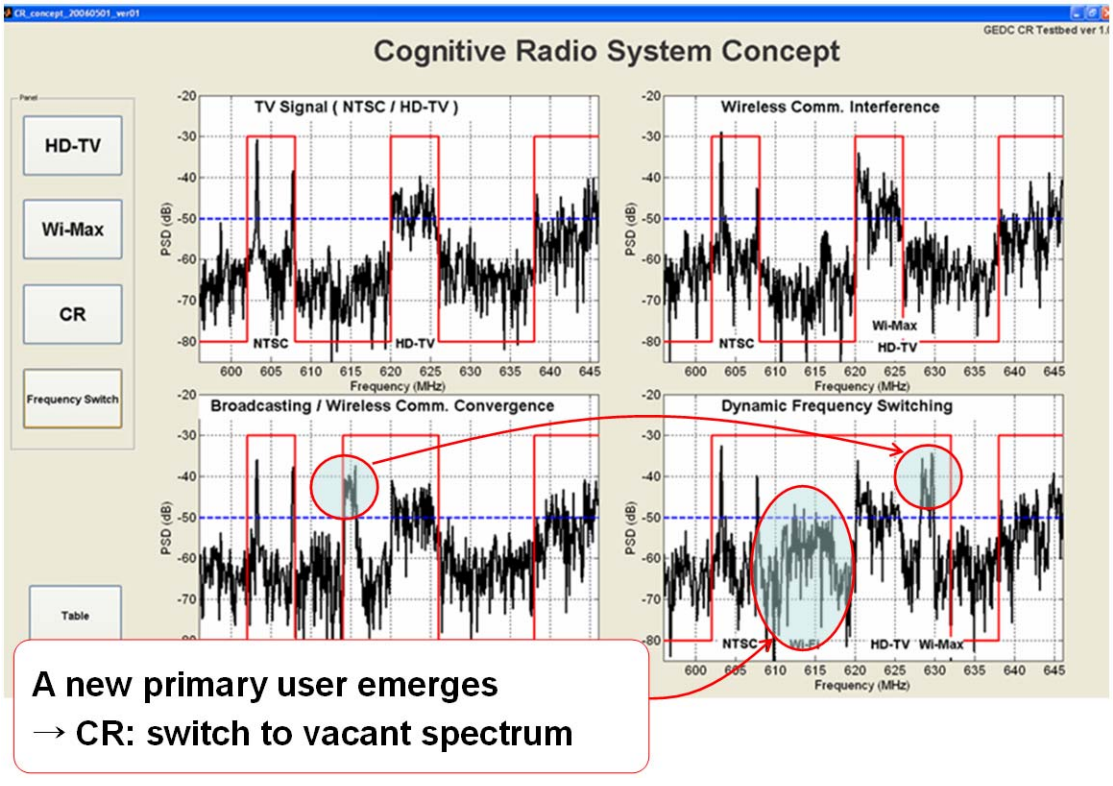


(b)

Figure 7. A GUI snapshot of a cognitive radio system concept demonstration.



(c)



(d)

Figure 7. continued.

(b) This is the case when spectrum sensing failed, and CR users try to use the same channel where a DTV signal is present. The CR user is assumed to use the WiMax standard signal with the 1.75-MHz bandwidth. At this time, the TV screen freezes because of the interference from the CR signal, and the CR signal also fails to communicate because of DTV signals.

(c) At this time, CR users succeeded in spectrum sensing and decided to use the vacant channel from 614 MHz to 620 MHz. Both TV and CR users get clear reception.

(d) This case shows the dynamic frequency switching, moving the CR signal to another vacant channel (from 626 MHz to 632 MHz) in the presence of another primary user (assumed to be a Wi-Fi signal) on the channel in which the CR has been used.

This demonstration shows the advantages of sharing spectrum resources and the necessity of spectrum sensing on CR systems.

2.3.2. Interference Analysis for UWB Coexistence with WiMax

The purpose of this demonstration is to analyze the effect of ultra wideband (UWB) over worldwide interoperability for microwave access (WiMax) as interference [9]. Although UWB is a promising wireless technology for the future with its high data rate, low power consumption and low cost, its worldwide acceptance is delayed by coexistence issues with other wireless standards such as WiMax [10], [11]. By using CR testbed, a quantitative interference analysis has been demonstrated to show desired-to-undesired (D/U) signal power ratio, being WiMax as the desired signal and UWB as the undesired signal.

In Figure 8, P_I is the interference signal power which is the UWB signal power in this case, P_N is the noise floor level, ΔP is the sensitivity decrement level, SNR_{REQ} is the minimum required signal-to-noise ratio (SNR) for a WiMax receiver to successfully demodulate the received signal, P_{TH} is minimum sensitivity of a WiMax receiver.

As the receiver recognizes the interference as noise, the overall noise level of the receiver will be increased by the power of the interference, which results in insufficient SNR for demodulation. Therefore, for each given ΔP, it is possible to set a limit of the permissible interference power as a function of ΔP.

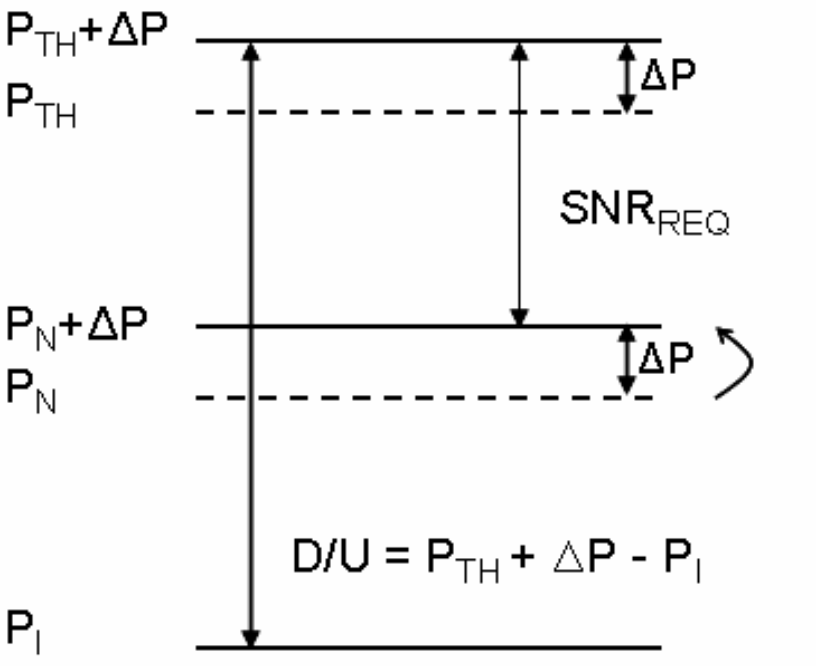


Figure 8. Signal and noise power diagram with interference.

With ΔP and P_I, the permissible D/U ratio of the receiver in the presence of interference is as follows.

$$D/U = P_{TH} + \Delta P - P_I$$
$$= SNR_{REQ} + \Delta P - 10\log_{10}\left(10^{\frac{\Delta P}{10}} - 1\right) \quad (1)$$

Therefore, by changing ΔP, it is possible to calculate the required D/U ratio as a function of input signal strength.

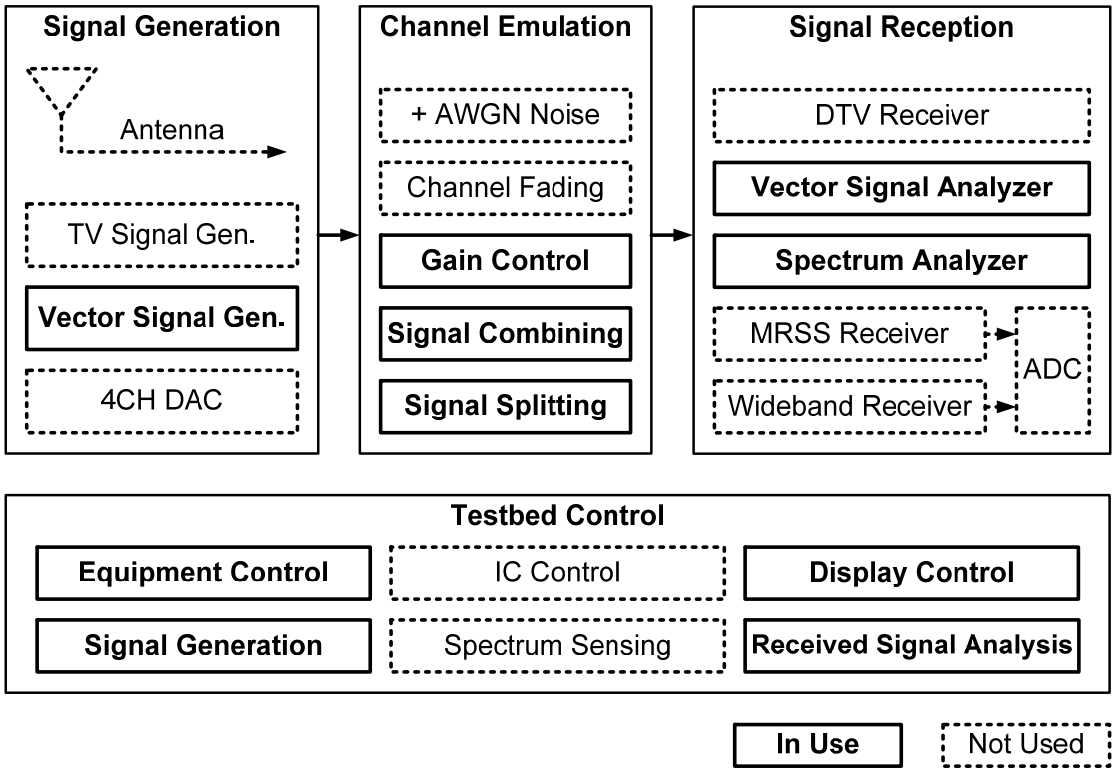


Figure 9. CR testbed configuration for interference analysis for UWB coexistence with WiMax.

Figure 9 shows the configuration of CR testbed for the verification of (1). Dual RF signals available from a vector signal generator emulate the victim-WiMax signal and interferer-UWB signals. These signals are combined together and fed into the vector signal analyzer to measure the WiMax signal quality. For WiMax signal generation, mandatory long length test message payload bit patterns are used, as defined in the WiMax standard

for measuring receiver sensitivity. The vector signal analyzer demodulates the WiMax signal from the combined signals and provides the spectrum, constellation, error vector magnitude (EVM), demodulated bit streams, and so on. Because bit error rate (BER) of 10^{-6} after forward error correction coding is a criterion of minimum WiMax sensitivity, the bit stream stored in a vector signal generator must be decoded to determine the BER. Customized MATLAB^{TM}-based software downloads the bit streams from a vector signal analyzer via Ethernet connection, then decodes the streams, and finally measures the BER. In accordance with the WiMax standard, the coding consisted of three parts: randomization, concatenated Reed-Solomon-convolutional coding, and interleaving.

The procedure for measuring permissible UWB interference starts with finding minimum sensitivity of WiMax without UWB interference. The minimum signal power level that satisfies a BER of 10^{-6} can be found by increasing the WiMax signal power from the lowest value. After the sensitivity measurement, the permissible UWB interference for a given WiMax power can be measured by finding the level which does not increase WiMax BER above 10^{-6}. The sweeping range of a WiMax power starts from minimum sensitivity. Measured WiMax sensitivity was -81 dBm/MHz. Figure 10 presents BER measurement results by sweeping UWB signal powers for the given WiMax power. For the experiments, WiMax, 64QAM, 3/4 coding rate, 7-MHz bandwidth signals are used.

Figure 11 shows the measured D/U ratio results from the experiments and calculated D/U ratio from (1). Although there are some level offsets between the two, the curves are very similar in shape and tendency. In general, the differences depend on the performance of equipments and channel selection filters. These results verify the proposed D/U ratio analysis approach.

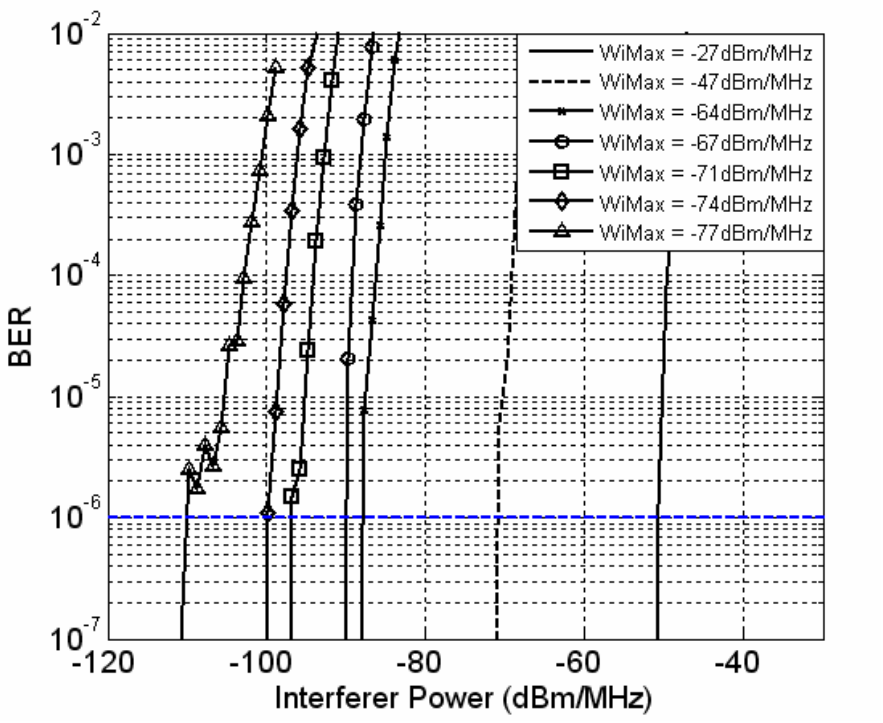


Figure 10. BER of WiMax with various signal power with UWB as an interferer.

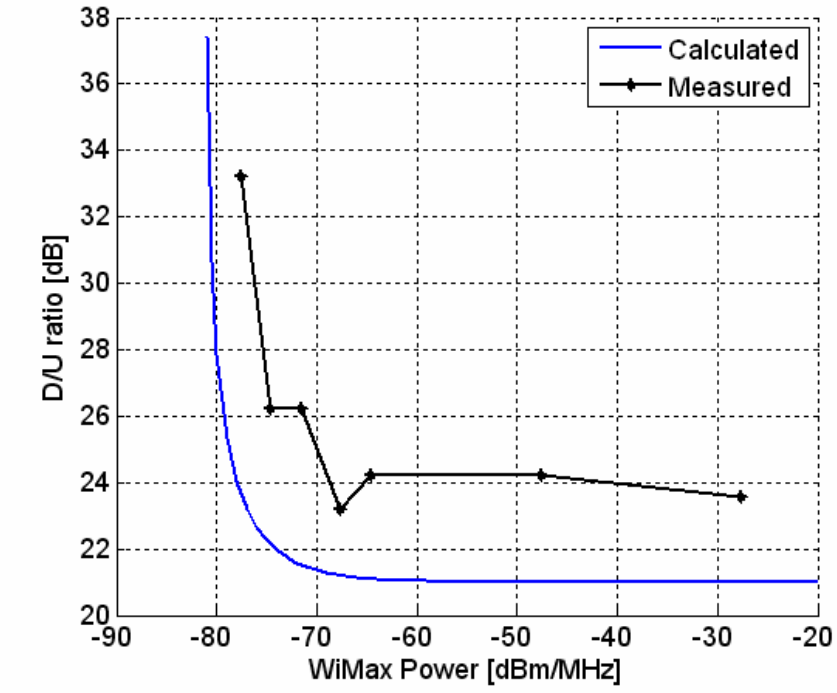


Figure 11. Calculated and measured D/U Ratio of a 64QAM-3/4, 7-MHz bandwidth WiMax signal with the presence of UWB as an interferer.

2.4. Summary

The cross-layer CR testbed has a flexible and scalable architecture for the versatile test of CR-related research. This testbed can be used from system-level concept verification to hardware custom-designed IC evaluation purposes. Its automated test procedure makes the evaluation repeatable and convenient. The testbed successfully showed the concept of the CR system and interference analysis of UWB over WiMax standard. In the following chapter, this testbed system is used for spectrum sensing IC evaluation. With this reconfigurable testbed, a new idea can be easily verified, demonstrated, and extended for further research.

CHAPTER 3

SPECTRUM SENSING TECHNIQUE

3.1. Spectrum Sensing Methods

Spectrum sensing technique is to find out the status of the current spectrum usage as accurate and fast as possible. So far, various spectrum sensing methods have been proposed. They can be categorized into two groups, i.e., feature detection [12] and energy detection [13].

Feature detection is designed to identify the unique signature features inherent in each signal modulation scheme, such as a preamble of an orthogonal frequency-division multiplexing (OFDM) signal or a pseudo-random noise (PN) sequence in a U.S. digital television (DTV) signal. Detection sensitivity of feature detection is usually higher than that of energy detection. However, it requires longer processing time and excessive digital hardware, substantially increasing power consumption.

In contrast, energy detection measures a total power within a certain frequency band and compares it with a threshold level to determine the presence of a signal. Although it is difficult for the energy detector to detect a signal below the noise level, this method provides faster sensing time and simpler implementation than those of feature detection. Moreover, since there is a trade-off between detection time and the detection bandwidth or the sensing threshold, it is possible to find a compromise between sensing time and accuracy. Given the wide variation in the signal bandwidth and formats that must be reliably sensed, it is preferable to have flexibility in selecting the detection bandwidth, just

as a spectrum analyzer that can adjust its resolution bandwidth depending on the frequency span and sweep time.

Table 2 summarizes the comparison between the feature detection method and the energy detection method.

Table 2. Comparison of the feature detection method and the energy detection method.

	Feature detection	Energy detection
Method	Identify unique signature features (preamble, PN sequence)	Measure the power within certain frequency band
Sensitivity	High	Low
Processing Time	Long	Short
Hardware Complexity	High	Low
Usage	Accurate, final sensing in a small bandwidth	Fast, initial sensing in a wide bandwidth

The IEEE 802.22 working group is developing a wireless regional area network (WRAN) standard based on CR technology utilizing the DTV broadcasting spectrum (i.e., VHF and UHF bands) [6], [14]. A dual-stage spectrum sensing scheme [15] was suggested to meet the requirements for sensing sensitivity and sensing time. Initially, an energy detector takes a snapshot of the current spectrum usage pattern over a wide bandwidth. In this stage, spectrum segments occupied by strong signals are identified and marked as occupied ones. Subsequently, a feature detector scrutinizes the unidentified candidate spectrum segments where signals from primary users are weak or absent. By applying feature detection methods only to the selected segments, total detection time can be significantly reduced while preserving the sensitivity requirement for spectrum sensing.

3.1.1. Conventional Energy Detection Methods

The conventional energy detection methods can be classified into the digital approaches [16] and the analog approaches [13], as shown in Figure 12.

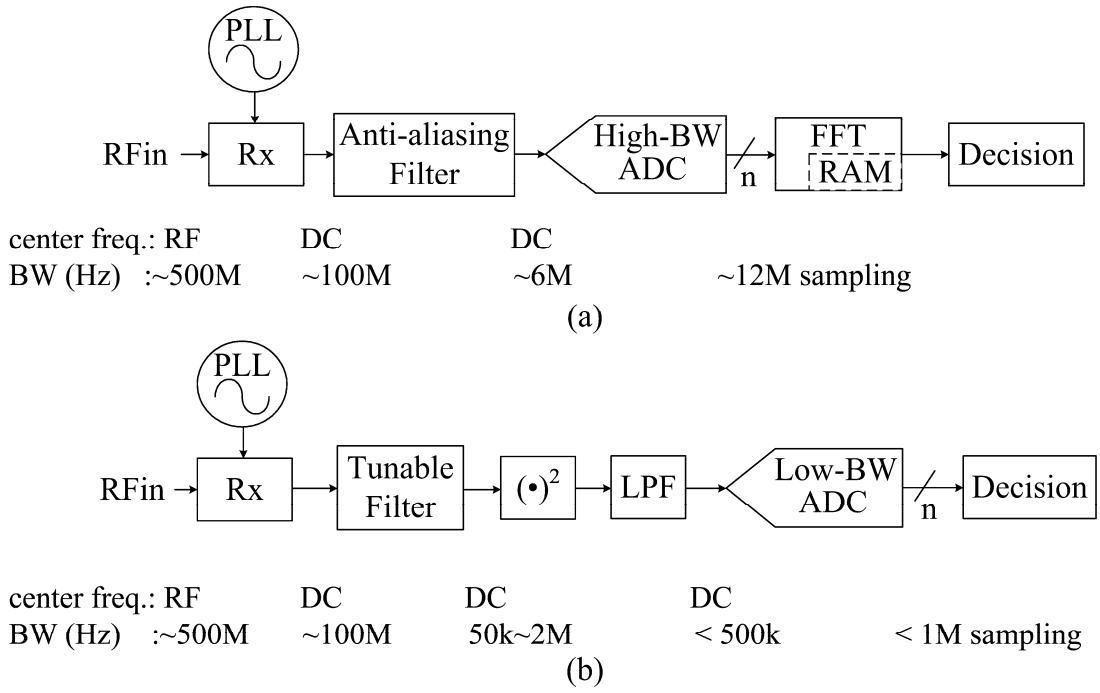


Figure 12. Conventional energy detection architectures; (a) the digital approach, and (b) the analog approach. The center frequency and the bandwidth are shown as an example.

A digital approach commonly uses a fast Fourier transform (FFT) block to calculate the power within each FFT bin by squaring its magnitude. In doing so, an ADC should have the sampling frequency of at least twice the input signal bandwidth. Therefore, compared with an analog approach, there are burdens on a digital approach with requirements for a high bandwidth ADC and complex digital FFT circuitry.

A conventional analog approach incorporates a squarer and a low-pass filter (LPF) to measure the signal power. The ADC bandwidth can be reduced because the signal power is

computed in the analog domain. In this case, the detection bandwidth can only be adjusted by using a tunable filter or filter banks in front of a squarer, so it tends to be bulky and difficult to integrate all the blocks.

To facilitate the commercialization of the CR transceiver, the spectrum sensing block must simultaneously provide sufficient tuning flexibility and detection accuracy in a small form factor that can be easily embedded into a transceiver system. However, conventional analog and digital approaches are insufficient in either accuracy, compactness, or tuning flexibility.

3.2. Proposed Feature Detection Technique

3.2.1. Overview of Analog Auto-correlation (AAC) Technique

Analog auto-correlation (AAC) is proposed as a feature detection method, using the beneficial properties of auto-correlation in the time domain [17]. This AAC technique enables identifying the unique signature feature of each specific signal type. Moreover, this feature detection technique in the time domain realizes simple and fast spectrum detection compared to conventional spectral feature detection methods.

Most of the communication signals have the periodic features, i.e., sinusoid carriers, periodic pulse trains, cyclic prefix, and preambles, etc. Each signal type has the corresponding unique feature (i.e., a signature) for a frame structure. A correlation process can derive the amount of the similarity between two signals, giving the maximum correlation for the same waveforms. Meanwhile, waveforms modulated with random data have little correlation between those waveforms. Therefore, the correlation between the periodic signal waveform and the data modulated signal waveform can be small enough to

be ignored. Using this benefit of the correlation characteristics, the periodic feature of the given signal can be a signature for a specific signal type.

Figure 13 shows the functional block diagram of the suggested AAC technique. The building blocks are composed of a delay line, a multiplier, and a sliding-window integrator. The input signal *r(t)* is delayed by certain time, T_d. This delay value T_d is a predetermined and unique value for each signal format. The correlation between the original input signal *r(t)* and the corresponding delayed signal $r(t-T_d)$ is performed by multiplying these two signals and integrating the resulting product. This correlation value is summed by the sliding-window integrator. When the resulting integrator output is greater than the certain threshold, the AAC sensing scheme determines the specific signal type for the input signal.

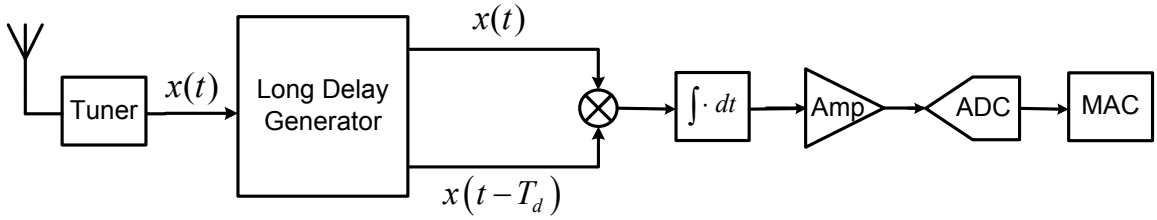


Figure 13. The conceptual block diagram of the proposed AAC.

This AAC process is performed in the time domain, enabling real-time operation and low power consumption. Compared with the spectral feature detection method [12], this temporal detection can reduce hardware burdens and power consumption for the signature feature detection because most of computation is done in the analog domain, thereby relaxing ADC requirements. To show the conceptual functionalities of the AAC technique, system simulations were performed with the IEEE 802.11a wireless local area network

(WLAN) standard signal. This WLAN signal has synchronization preambles at the beginning of each frame, consisting of ten short preambles, each lasts 0.8 μsec and two long preambles, each lasts 3.2 μsec, as shown in Figure 14.

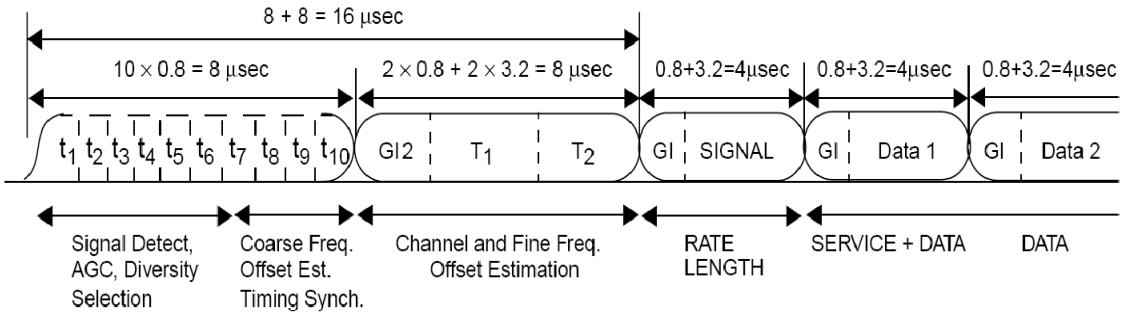
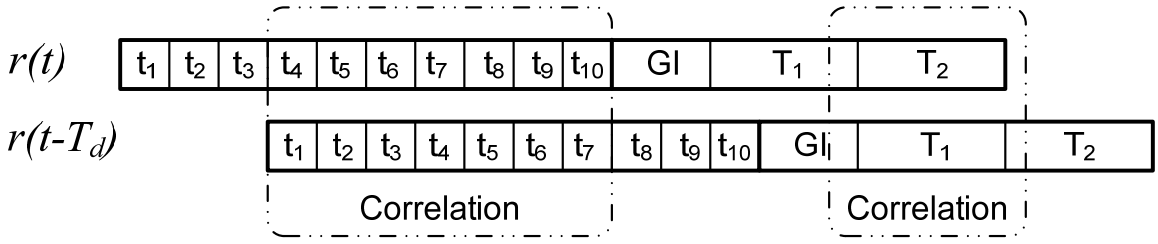


Figure 14. The frame structure of an IEEE 802.11a WLAN signal.

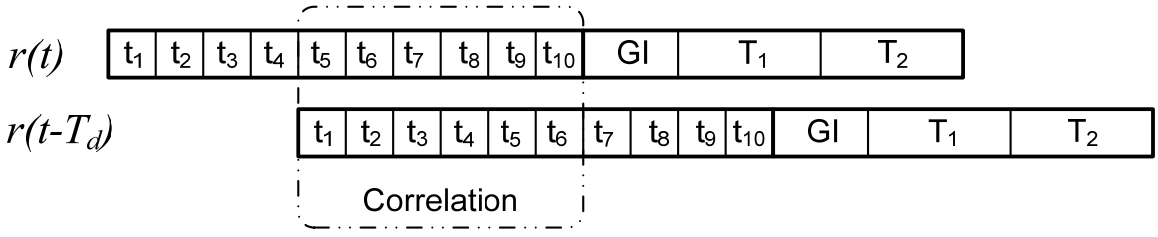
Figure 15 shows the conceptual correlation timing diagram of AAC operations. Figure 15(a) is the case when the time delay is 3.2 μsec. Then, seven short preambles and one long preamble will be overlapped between the original signal and the delayed signal. Those overlap will create a strong correlation, while other signals would not highly correlated. Figure 15(b) is the case when the time delay is 4.0 μsec. Then, six short preambles will be overlapped between the original signal and the delayed signal, creating a strong correlation. In sum, for the IEEE 802.11a signal, multiples of 0.8 μsec will create at least one high correlation value, depending on delay time, T_d.

Figure 16 shows the case when the time delay, T_d, is 3.2 μsec. The original input signal $r(t)$ and the delayed signal $r(t-T_d)$ are shown in Figure 16(a) and Figure 16(b), respectively. For the correlation, those two signals are multiplied and go through sliding-window integrator, as shown in Figure 16(c) and Figure 16(d), respectively. The resulting

correlation waveform has the repeating positive values for each overlap of preambles. The resulting sliding-window integrator output has peak values for each preamble location within the IEEE 802.11a frame structure, as shown in Figure 15(a). Meanwhile, the correlation for the modulated data symbols has the random values and becomes small after the sliding-window integration. By comparing the predetermined threshold with the resulting waveform shown in Figure 16(d), the AAC technique determines reception of the IEEE 802.11a - OFDM signal.



(a)



(b)

Figure 15. Conceptual correlation timing diagram for AAC with (a) T_d = 3.2 μsec and (b) T_d = 4.0 μsec.

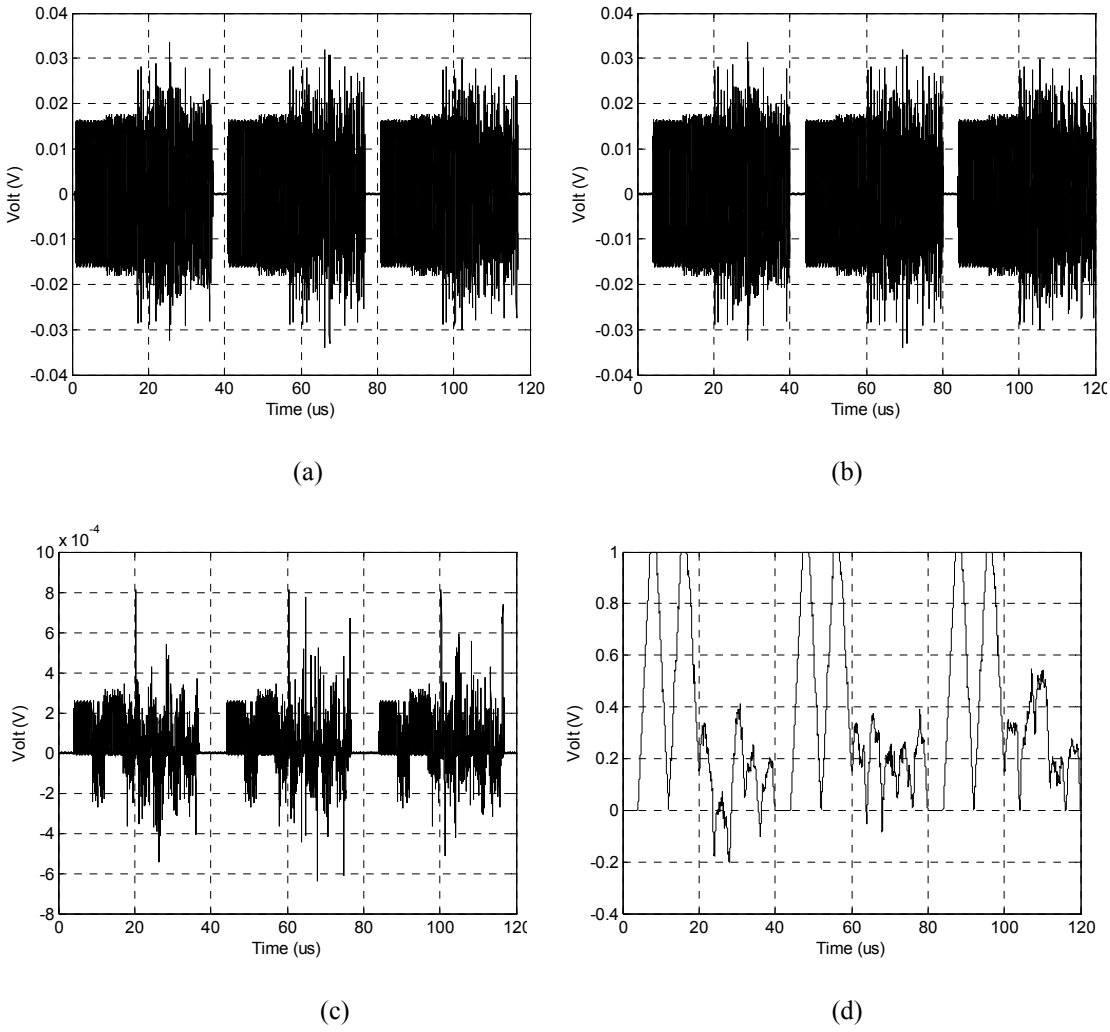


Figure 16. Simulation results of AAC with T_d = 3.2 μsec. (a) The original signal, *r(t)*, (b) the delayed signal, $r(t-T_d)$, (c) multiplier output, $r(t)\times r(t-T_d)$, and (d) sliding-window integrator output, $\int r(t)\times r(t-T_d)dt$ from *0* to T_d.

Figure 17 shows the case when the time delay, T_d, is 4.0 μsec. From Figure 15(b), it is clear that the correlation will be high only for the overlapped short preambles, which is shown as a peak in Figure 17(d). Therefore, by changing the time delay to the predetermined value specific for a certain signal type and observing the correlation output, the type of an input signal can be identified.

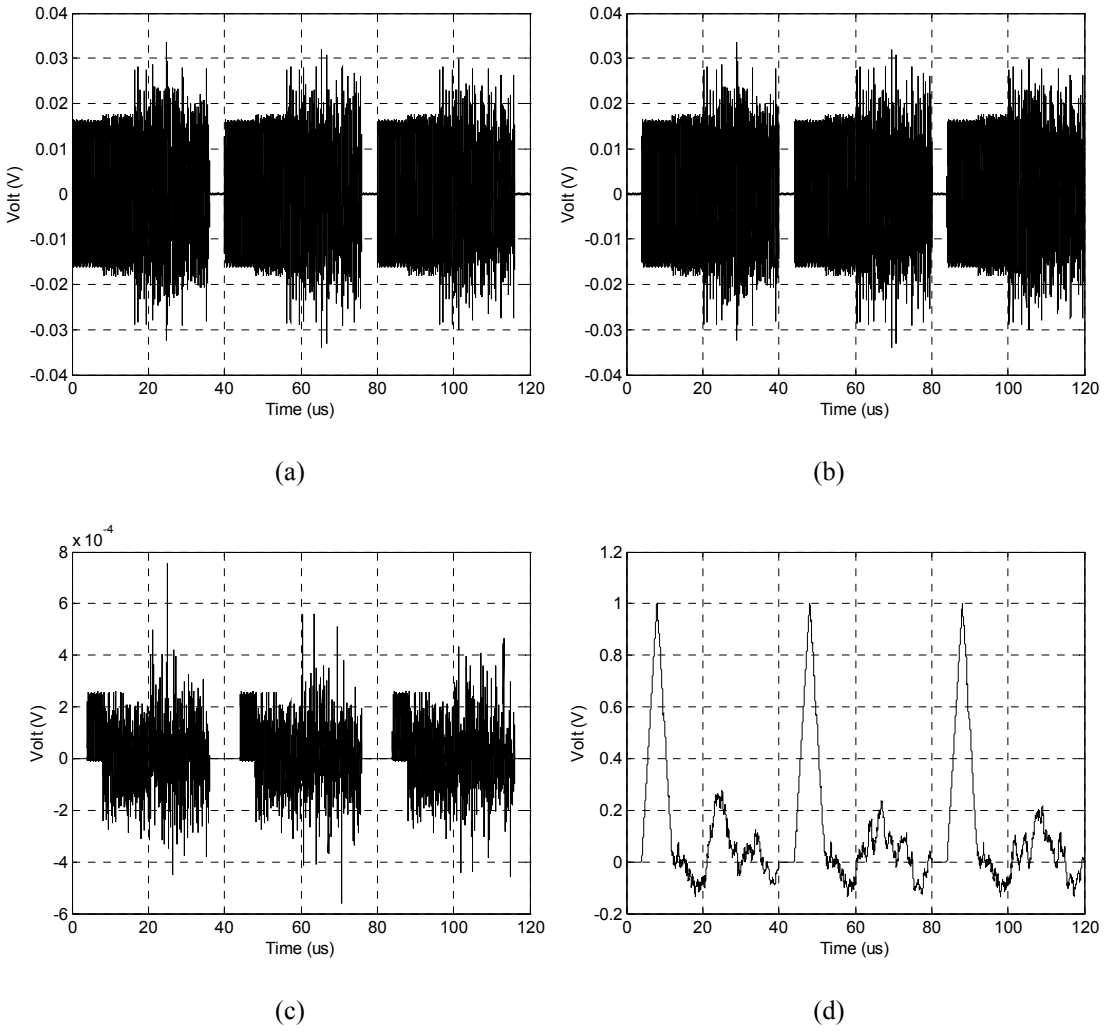


Figure 17. Simulation results of AAC with T_d = 4.0 μsec. (a) The original signal, *r(t)*, (b) the delayed signal, $r(t-T_d)$, (c) multiplier output, $r(t)\times r(t-T_d)$, and (d) sliding-window integrator output, $\int r(t)\times r(t-T_d)dt$ from *0* to T_d.

3.2.2. Long Delay Generation for AAC

In implementing AAC, the key requirement is to generate the delayed RF signal by a pre-defined time delay, T_d. The value of T_d depends on which standard to detect, but ranges from a few nano-seconds to the order of micro-seconds. Implementing this amount of delay in an analog fashion is extremely hard.

The long delay generator provides for arbitrary long delay without corrupting the auto-correlation property of the signal. The proposed long delay generator includes an ADC, memory element, and a DAC. The memory element can be implemented with either shift register bank or random access memory (RAM) cells, as will be described in further detail below. By delaying the signal in the digital domain, the quality of the signal is solely determined by the ADC and DAC. That is, the process of delay does not degrade the quality of the signal, no matter how long the delay is made. Therefore, an arbitrary long delay can be made without corrupting the signal. The minimum achievable delay step is determined by the clock speed, and the maximum achievable delay amount is determined by the size of the memory element. The regeneration of the delayed signal into the analog domain ensures the low-power operation and real-time computation, compared with the auto-correlation computation in the digital domain.

Figure 19 shows the long delay generator using shift register bank, which consists of an ADC, shift register bank, addressing circuitry, and two DACs. The sampling frequency of the ADC, f_s, determines the unit delay, T_{ud}, of the shift register bank. The resolution of the ADC can be equal to the bit-width of the shift register bank and the resolution of the DAC. The input, $x(t)$, is sampled and digitized with the ADC at every clock rising edge, producing $x'(t)$. At the same time, the digitized input signal $x'(t)$ is stored in the first column of the shift register bank. At every clock rising edge, the shift register bank moves the data from the preceding column to the next column. The desired position of the output can be calculated as $n = T_d / T_{ud}$. The output of the n^{th} column of the shift register bank is $x'(t-n \cdot T_{ud})$. Once the position n is calculated, the addressing circuitry selects the output of n^{th} register column to the input of the DAC. The other DAC input is connected to the first

register column output. By using two identical DACs, which will be triggered with the same clock signal, the quality of the regenerated signals *x"(t)* and *x"(t-n·T_{ud})* can be equivalent each other, thus having the minimum effect on the subsequent auto-correlation calculation.

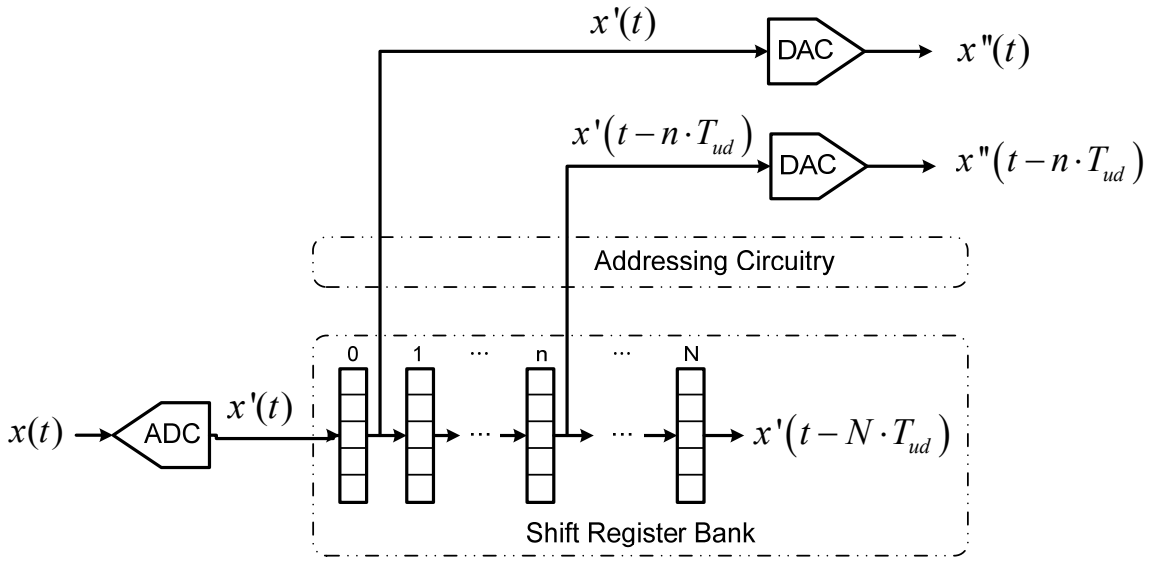


Figure 18. Possible implementation examples of the long delay generation using shift register bank.

Figure 19 shows the alternative implementation method for the long delay generation using RAM, consisting of an ADC, RAM, memory controller, and two DACs. At every clock edge, the digitized input signal *x'(t)* is stored in the arbitrary row of the RAM, which can be determined by the memory controller. The memory controller determines the next storage position, or the row address. For example, the memory controller can start with the bottom of the RAM and simply increase the row address in a sequential manner, as shown in Figure 19.

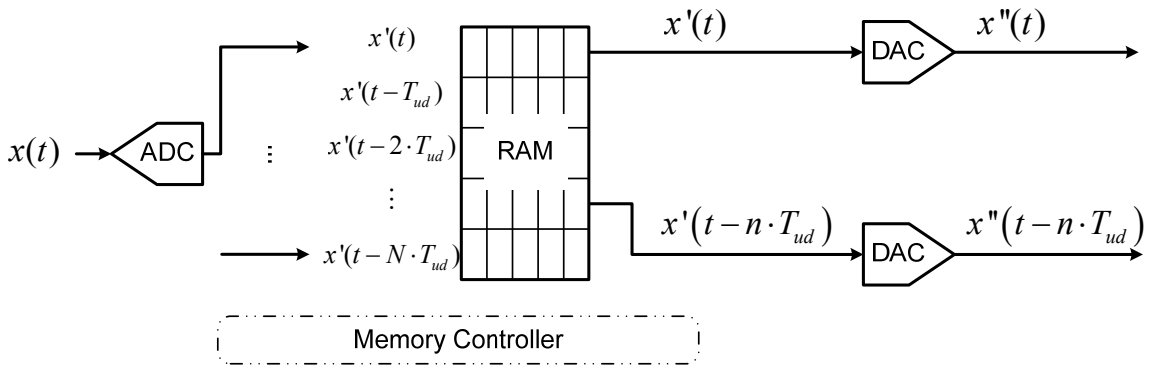


Figure 19. Possible implementation examples of the long delay generation using RAM.

By using shift register banks as a memory element of the long delay generator, the addressing circuitry may be simpler compared when the RAM is used as a memory element of the long delay generator. The shift register bank does not require an input addressing block because the input always goes to the first register bank. Moreover, one input of the DAC may be hard-wired to the output of the first register bank. The addressing circuitry may only choose the input of another DAC among *N* outputs of each register. When the RAM is utilized, on the other hand, the input of the RAM as well as the output should be controlled via adequate addressing, requiring relatively complex memory controller. However, the unit storage element of the RAM may occupy smaller area and consume less power than that of shift register bank, thus having advantage when the required size of the memory element is large.

3.3. Proposed Energy Detection Technique

The multi-resolution spectrum sensing (MRSS) technique is proposed as an energy detection method that uses the correlation of the received signal and the internally generated window signal. The window is generated with digital circuitry, while the

computation is done in the analog domain. In sum, it is a digitally assisted analog energy detection method.

3.3.1. Windowing Effect

To eliminate the need for a tunable filter in a receiver chain, MRSS adopted the concept of windowing received signals. Windows have been widely used in discrete-time signal processing before applying a fast Fourier transform (FFT) to reduce the spectral leakage associated with finite observation intervals [18]. Windows have the time-frequency localization property, so the multiplication of their time duration and frequency bandwidth is constant [19]. Among various windows, a Gaussian window is the most localized one between the time and frequency domain, having a minimum time-bandwidth product, as shown below:

$$\Delta_t \Delta_\omega = \frac{\sigma}{\sqrt{2}} \times \frac{1}{\sqrt{2}\sigma} = \frac{1}{2} \tag{2}$$

where Δ_t and Δ_ω represent the signal's energy spread in the time and frequency domain, respectively, and σ is the standard deviation of the Gaussian window. Although it has a minimum time-bandwidth product, infinite time is required to produce an accurate Gaussian window. Therefore, other time-confined windows such as a Hann or Hamming window are frequently used. In the case of the Hann window, $\Delta_t \Delta_\omega$ equals 0.5131 [19]. The virtue of this localization is that the bandwidth of the window can be adjusted by merely changing the duration of the window. Windows have a low-pass filtering characteristic, and their bandwidth is inversely proportional to the duration of the window. In other words,

a short window in the time domain has a wide bandwidth in the frequency domain, and a long window has a narrow bandwidth.

Figure 20(a) shows various $\cos^{\alpha}(\pi f_{\omega} t)$ windows in the time domain, where α is the order of the window, and f_{ω} is the window frequency, which is the same as the inverse of the duration of the window, t_{ω}. Figure 20(b) is the log-scale magnitude response in the frequency domain. When α is two, it is usually called a Hann window. As f_{ω} is decreased from 1 MHz to 100 kHz with the same α of two, the duration of the window is increased from 1 μsec to 10 μsec, and the bandwidth of the window is decreased by a factor of 10. Table 3 summarizes the figures-of-merit (FOM) of various $\cos^{\alpha}(\pi f_{\omega} t)$ windows. Among them, the equivalent noise bandwidth is the bandwidth of an ideal rectangular filter with the same peak gain that would accumulate the same noise power from white noise as does the window, thereby indicating the bandwidth of a window. As α increases, the side-band roll-off becomes steeper, meaning the selectivity is improved at the expense of a slightly increased bandwidth [18].

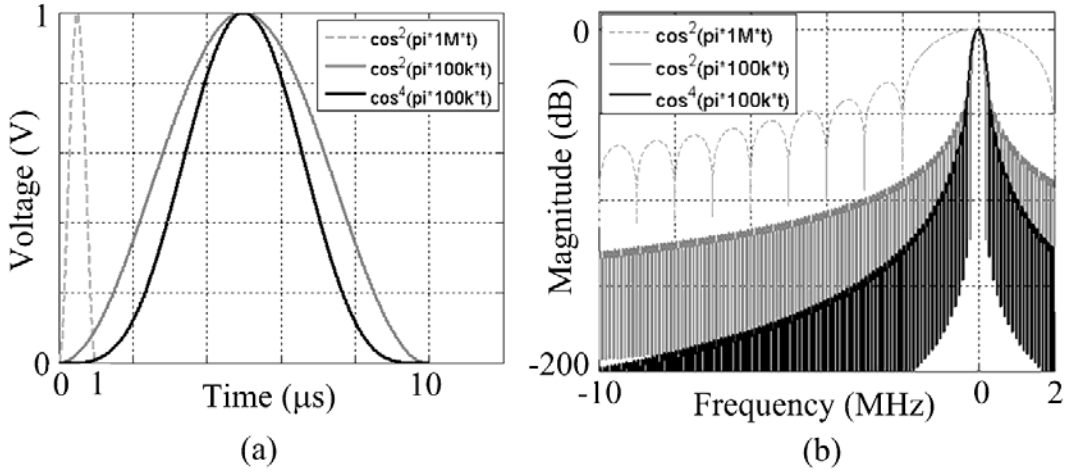


Figure 20. $\cos^{\alpha}(\pi f_{\omega} t)$ window characteristic, (a) in the time domain, and (b) in the frequency domain.

Table 3. Figures of merit of $\cos^{\alpha}(\pi f_{\omega} t)$ windows.

Window	Highest Sidelobe (dBc)	Equiv. Noise BW (Hz)	3-dB BW (Hz)
$\cos(\pi f_{\omega} t)$	-23	$1.23\, f_{\omega}$	$1.20\, f_{\omega}$
$\cos^2(\pi f_{\omega} t)$	-32	$1.50\, f_{\omega}$	$1.44\, f_{\omega}$
$\cos^3(\pi f_{\omega} t)$	-39	$1.73\, f_{\omega}$	$1.66\, f_{\omega}$
$\cos^4(\pi f_{\omega} t)$	-47	$1.94\, f_{\omega}$	$1.86\, f_{\omega}$

3.3.2. MRSS Overview

Suppose *w(t)* is a real window that is time-confined to t_{ω} and symmetric, as defined in (2), and *r(t)* is a downconverted baseband signal. Then, the correlation of *w(t)* and *r(t)* in the time domain corresponds to multiplication in the frequency domain, resulting in a filtering effect by the low-pass filtering characteristic of a multiplied window, as shown in (3) and (4), where $\star$ denotes the cross-correlation operator.

$$w(t) = \begin{cases} w(t_{\omega} - t), & \text{if } 0 < t < t_{\omega} \\ 0, & \text{elsewhere} \end{cases} \tag{3}$$

$$(w \star r)(x) = \int_{-\infty}^{\infty} w^*(t) r(x+t) dt = \int_{-\infty}^{\infty} w(t) r(x+t) dt = \int_{-\infty}^{\infty} W(f) R(f) e^{j2\pi fx} df \tag{4}$$

$$(w \star r)(0) = \int_{-\infty}^{\infty} w^*(t) r(t) dt = \int_{-\infty}^{\infty} w(t) r(t) dt = \int_{0}^{t_{\omega}} w(t) r(t) dt = \int_{-\infty}^{\infty} W(f) R(f) df \tag{5}$$

Figure 21 shows the concept of correlation to capture the signal power within the window bandwidth. Figure 21(a) is the case when the signal frequency is within the window bandwidth, so the correlation result is large. On the other hand, Figure 21(b) is the

case when the signal frequency is outside of the window bandwidth, so the degree of correlation is small.

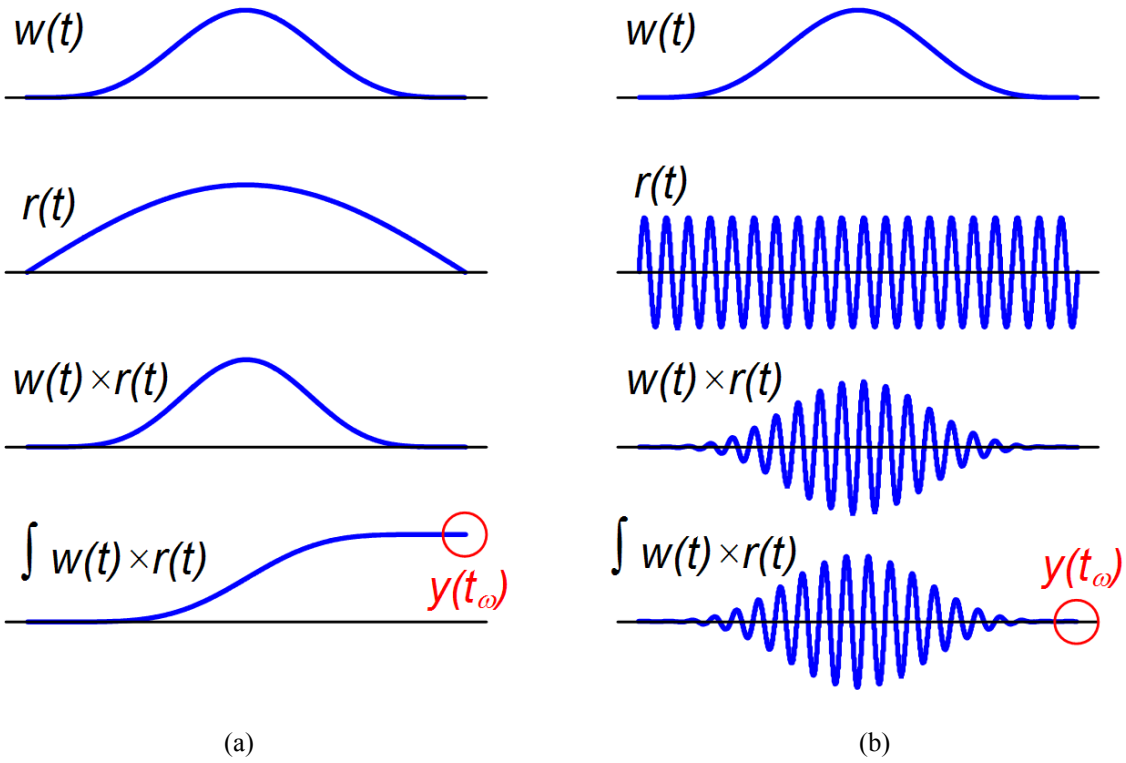


Figure 21. Correlation examples when (a) the signal frequency is within the window bandwidth, and (b) the signal frequency is outside of the window bandwidth.

The MRSS technique utilizes the time-frequency localization of a window to provide programmable bandwidth control. In other words, the variation of window type and window duration will change the detection bandwidth without using a tunable filter. Such a flexible window is generated in the digital domain by a digital window generator (DWG) block. The DWG consists of a random-access memory (RAM), a digital-to-analog converter (DAC), and a low-pass filter (LPF). The RAM stores any kind of window data, and the DAC and the LPF reconstruct the window signal with a variable duration. Figure

22 shows a simplified block diagram of MRSS. The correlator output is sampled by a low-bandwidth analog-to-digital converter (ADC), and the detection decision is performed in the digital domain. In summary, MRSS is a digitally assisted analog energy detector without an extra analog filter.

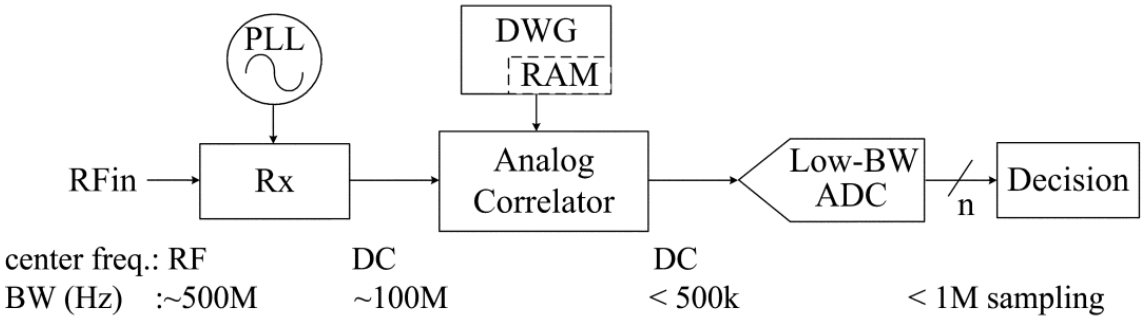


Figure 22. A simplified architecture of the MRSS system. The center frequency and the bandwidth are shown as an example.

Total sensing time in performing MRSS can be calculated as

$$t_{total} = \left(\frac{f_{end} - f_{start}}{f_{step}} + 1 \right) \times \left[N_{AVG} \left(t_{\omega} + t_{buf} \right) + t_{sw} \right] (\text{sec}) \tag{6}$$

where $(f_{end} - f_{start})$ is the frequency sweep range of the phase locked loop (PLL), f_{step} is the amount of frequency change in PLL, N_{AVG} is the number of averages at one PLL frequency, t_{buf} is a margin between consecutive windows, t_{ω} is the window duration as defined in (2), and t_{sw} is maximum switching settling time of the PLL. The draft of the IEEE 802.22 specification demands channel sensing time to be completed in less than two seconds [14]. Total sensing time can be varied significantly depending on how sensing is done and what kind of a signal is to be detected. MRSS is proposed as one of the energy detection methods, so it aims to have fast sensing by compromising sensitivity that can be adjusted by the type

and duration of a window. For example, if a 100-kHz window is used with 100 averages, t_ω is 10 µs, t_{buf} is 1.67 µs, N_{AVG} is 100, and t_{sw} is 300 µs. Therefore, total sensing time will be 1.467 ms times the number of frequency sweeps. If the U.S. DTV signal is to be detected, sensing of one channel can be done just by looking at the pilot signal [14], so the number of sweeps can be one per channel.

Figure 23 shows the multi-resolution property of MRSS with two window frequencies, one with f_ω = 100 kHz and the other with f_ω = 1 MHz. The inputs to this simulation are a continuous wave (CW) signal of -50 dBm at 582 MHz, an advanced television systems committee (ATSC) signal of -30 dBm at 600 MHz, and a digital video broadcasting - terrestrial (DVB-T) signal of -70 dBm at 615 MHz. ATSC uses eight-level vestigial sideband (8-VSB) modulation, and DVB-T uses the orthogonal frequency-division multiplexing (OFDM) modulation scheme.

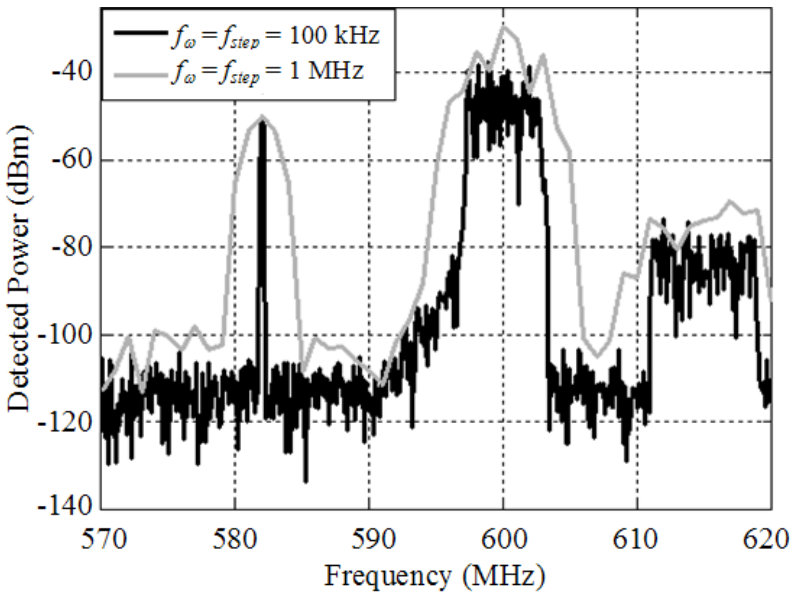


Figure 23. Fine (f_ω = 100 kHz) and coarse (f_ω = 1 MHz) resolution property of MRSS using the $\cos^4(\pi f_\omega t)$ window. Inputs are CW (-50 dBm @ 582 MHz), ATSC (-30 dBm @ 600 MHz), and DVB-T (-70 dBm @ 615 MHz).

From Figure 23, it is evident that the duration change affects the resolution of MRSS. Coarse resolution gives only a glimpse of the spectral usage, but it can be done in a fast way. On the other hand, fine resolution MRSS provides a more precise result as well as a reduced noise floor level. The level difference between the detected power and the input power of ATSC and DVB-T is because of the effective bandwidth of the window.

3.3.3. Advantages over Conventional Approaches

There are several advantages of MRSS over conventional approaches.

Compared with the conventional digital approach, MRSS substantially relaxes the ADC's bandwidth requirement and power consumption, and its initial output latency can be smaller than that of the digital approach. The hardware requirements of an $N(=2^n)$-point FFT of various algorithms can be found in [20]. Because the input and the immediate results should be reordered during FFT, there should be a memory with a size of around N words, which is comparable to the RAM size of the DWG. The complexity of digital multipliers and adders for the digital approach could correspond to that of the DAC, LPF, and the analog correlator in MRSS. However, the ADC bandwidth requirement of the MRSS can be reduced by one order of magnitude than that of the digital approach, which will contribute to the reduction of power consumption. Sensing time of the digital approach highly depends on how the FFT block is implemented, especially the sampling frequency, f_{clk}, and the FFT size, N. Because of the accumulation of the input signal for the FFT and the use of a pipelined structure, the initial latency of FFT computation is usually $N+k \cdot log_2 N$ clock cycles, where k depends on how FFT blocks are pipelined [20]. For energy detection, it is common to fix N to the finest resolution of f_{clk}/N and control its detection bandwidth to

be $f_{clk} \cdot M/N$, where M is the number of adjacent bins averaged together [16]. Therefore, bandwidth control does not change the output latency, and the output latency is longer than required except for M=1. Accordingly, the output latency of the digital approach is the sum of FFT processing time, power computation time of the FFT output, and averaging time of M bins. If a windowing is adopted before the FFT to reduce the spectral leakage [18], it will further increase the output latency. Meanwhile, the output latency of MRSS is the sum of analog processing time, t_{ω}, and power computation time.

In contrast to the conventional analog approach, MRSS does not require any analog filters in the RF signal path. Because MRSS has more flexibility in bandwidth adjustment without the additional hardware overhead, it can be implemented in a smaller form factor, thus reducing the fabrication cost. While the bandwidth of an analog tunable filter usually has a variation because of the process, supply voltage, and operating temperature (PVT), the detection bandwidth of MRSS is immune to such variations because the window is controlled by the reference clock, which is usually the most accurate signal in the integrated circuit (IC).

Table 4 summarizes the comparison of the MRSS technique with other conventional approaches.

Table 4. Comparisons of the MRSS technique with other conventional approaches.

		MRSS	Digital approach	Analog approach
Signal processing unit		analog correlator	digital FFT + squarer	analog squarer + LPF
ADC requirement		< 1 Msps 7 bit	~ 10 Msps 7 bit	< 1 Msps 7 bit
ADC anti-aliasing filter		No	yes	no
Detection BW, f_{BW}		window BW	f_{clk} / FFT size	tunable filter BW
Detection BW reference		Clock	clock	tunable filter
Circuit complexity	Analog	mid.	high (ADC)	high
	Digital	mid.	high	low
Processing		Serial	parallel	serial
Output latency		Small	large	small

CHAPTER 4

SENSING THRESHOLD DETERMINATION OF MRSS TECHNIQUE

4.1. Sensing Threshold Model

4.1.1. Spectrum Sensing Scenario

The goal of spectrum sensing is to find whether the specific spectrum channel is occupied by primary users or not. Therefore, binary hypothesis testing with two hypotheses of (7) and two decisions of (8) can be used [21]. The decision is done by comparing the detected signal power, P_{MRSS}, with the sensing threshold, P_{TH}, as shown in Figure 24 and Figure 25.

$$\begin{cases} H_0 : \text{ Channel is vacant} \\ H_1 : \text{ Channel is occupied} \end{cases} \tag{7}$$

$$\begin{cases} D_0 : \text{ Channel is vacant} \\ D_1 : \text{ Channel is occupied} \end{cases} \tag{8}$$

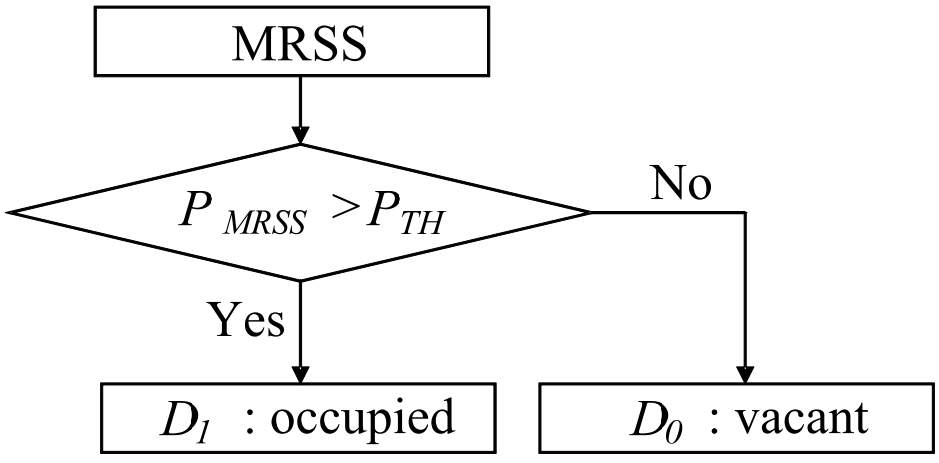


Figure 24. MRSS decision process.

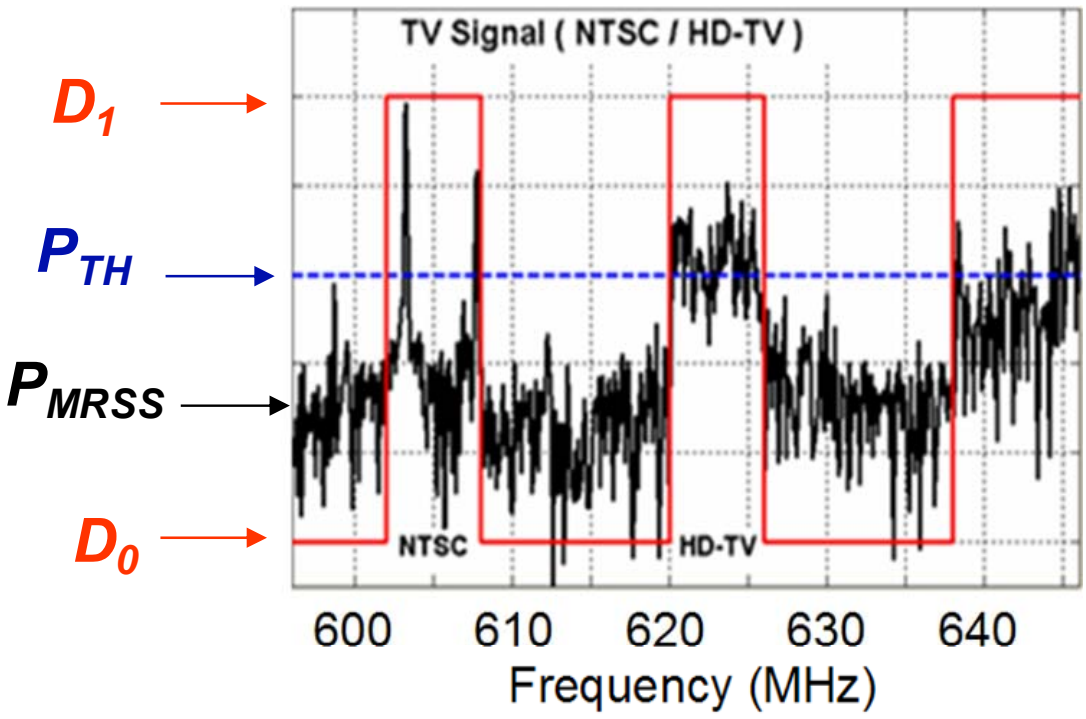


Figure 25. MRSS decision example with TV signals.

Three probabilities of interest are the probability of false alarm, P_{FA}, the probability of misdetection, P_M, and the probability of detection, P_D. P_{FA} is the probability of deciding the channel is occupied when it is actually vacant. On the other hand, P_M is the probability of deciding the channel is vacant when it is in fact occupied. In addition, P_D is the desired detection probability when the signal is present.

$$P_{FA} = P(D_1 \mid H_0) \tag{9}$$

$$P_M = P(D_0 \mid H_1) \tag{10}$$

$$P_D = 1 - P_M \tag{11}$$

The occupancy decision is made by comparing the MRSS result and the pre-defined sensing threshold level, P_{TH}. Too high of a threshold will give a low false alarm, but the detection probability will decrease. On the other hand, too low of a threshold would result

in an increase of false alarm rate. Therefore, the threshold level should be based on the acceptable false alarm rate, P_{FA}. For example, if the accepted false alarm rate is 0.1, the threshold level should be set to the point where P_{FA} reaches 0.1. As shown in (9), false alarm rate is based on the MRSS result when there is no signal in the channel of interest. Therefore, the determination of the threshold level is affected by the MRSS result distribution on noise power detection.

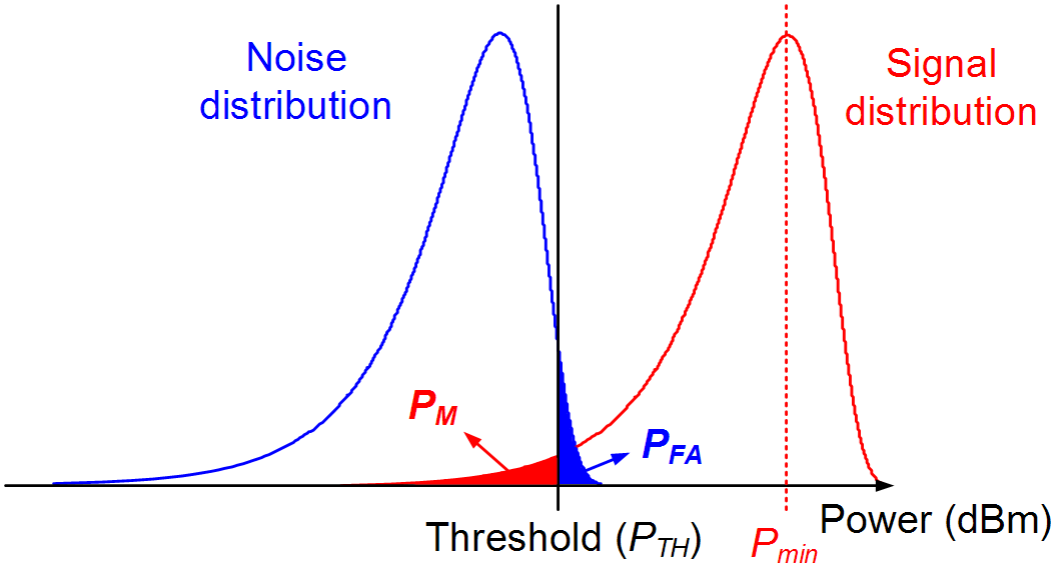


Figure 26. Graphical representation of the probability of misdetection, P_M, the probability of false alarm, P_{FA}, sensing threshold, P_{TH}, and the minimum detectable signal power, P_{min}.

4.1.2. The Statistical Distribution of MRSS on the Noise Power

The envelope voltage of white Gaussian noise has a Rayleigh distribution with its power density function (PDF) of $f_v(v)$, as shown in (12) [22].

$$f_v(v) = \begin{cases} \frac{v}{\sigma^2}\exp\left(-\frac{v^2}{2\sigma^2}\right), & \text{if } v \geq 0 \\ 0, & \text{if } v < 0 \end{cases} \tag{12}$$

If the envelope voltage is expressed in a logarithmic domain, especially in a dB scale, the new variable $x = 20log(v)$ would have a PDF of $f_X(x)$, mean μ_x and standard deviation σ_x, as shown in (13)-(15), respectively [23]. It is sometimes referred to as a log-compressed Rayleigh distribution.

$$f_X(x) = \frac{1}{10\log(e)}\exp\left[\frac{x}{10\log(e)} - \ln(2\sigma^2) - \exp\left(\frac{x}{10\log(e)} - \ln(2\sigma^2)\right)\right] \tag{13}$$

$$\mu_x = 10\log\left(\frac{2\sigma^2}{\exp(\gamma)}\right)(dBV),\ \gamma \approx 0.5772 : \text{Euler-Mascheroni constant} \tag{14}$$

$$\sigma_x = \frac{10\pi\log(e)}{\sqrt{6}} = 5.57(dB) \tag{15}$$

One way of reducing the variation on the detected noise power is to average the individual detection results [22]. If this averaging is done in a logarithmic domain, the resultant PDF of $f_{X,AVG}(x)$, mean of μ_{AVG}, and standard deviation of σ_{AVG} by averaging N_{AVG} independent measurements are

$$f_{X,AVG}(x) = \frac{\sqrt{N_{AVG}}}{10\log(e)}\exp\left[\frac{\sqrt{N_{AVG}}}{10\log(e)}x - \ln(2\sigma^2) - \exp\left(\frac{\sqrt{N_{AVG}}}{10\log(e)}x - \ln(2\sigma^2)\right)\right] \tag{16}$$

$$\mu_{AVG} = 10\log\left(\frac{2\sigma^2}{\exp(\gamma)}\right)(dBV),\ \gamma \approx 0.5772 : \text{Euler-Mascheroni constant} \tag{17}$$

$$\sigma_{AVG} = \frac{10\pi\log(e)}{\sqrt{6N_{AVG}}} = \frac{5.57}{\sqrt{N_{AVG}}}(dB). \tag{18}$$

With the statistical information on the noise distribution, the sensing threshold can be calculated for the given false alarm rate. Moreover, based on the given sensing threshold, the probability of misdetection can be estimated. From (18), larger number of averaging results in less variation of noise. Therefore, it is expected to reduce the false alarm rate at a given sensing threshold, or to lower the threshold for a given false alarm rate.

4.1.3. The Threshold Level Determination

The threshold level decision may begin with noise floor estimation. Let the input-referred noise figure of the MRSS receiver path be *NF* in a dB scale. The window with the window frequency of f_w will have an equivalent noise bandwidth of f_{NBW}. Table 3 shows some f_{NBW} values for various $\cos^{\alpha}(\pi f_w t)$ windows. f_{NBW} is proportional to f_w and a window-specific factor. The actual average power of the noise floor will be

$$\mu = -174 + NF + 10\log\left(f_{NBW}\right)(dBm). \tag{19}$$

The true power of Rayleigh distribution voltage with variance of σ^2 is as below [10].

$$\overline{P} = \int_0^{\infty}\left(\frac{V^2}{R}\right)\left(\frac{V}{\sigma^2}\exp\left(-\frac{V^2}{2\sigma^2}\right)\right)dv = \frac{2\sigma^2}{R} \tag{20}$$

From (14), the log-compressed Rayleigh distribution represents an average power as follows;

$$\overline{P_{LR}} = \frac{\overline{V_{LR}^2}}{R} = \frac{10\,\hat{}\,(\mu_x/10)}{R} = \frac{2\sigma^2}{\exp(\gamma)R.} \tag{21}$$

Thus, the difference between those two is

$$\overline{P_{LR}}\Big|_{dB} - \overline{P}\Big|_{dB} = -\frac{10\gamma}{\ln(10)} = -2.507dB. \tag{22}$$

Therefore, signal processing of the envelope voltage of white Gaussian noise in a logarithmic domain causes an under-response of -2.51 dB compared with the true noise power. If the result of MRSS is processed in a logarithmic domain, the detected noise power will have an under-response of -2.51 dB. Therefore, the detected noise floor becomes

$$\mu_N = -174 + NF + 10\log\left(f_{NBW}\right) - 2.51 \ (dBm). \tag{23}$$

Thus, the detected noise floor is a function of system noise figure and the duration and the shape of the window. Decreasing the duration of the window will increase the speed of MRSS, but at the expense of the increased noise floor and the decreased resolution. With the same duration of the window, the shape of the window will affect the detected noise floor, but the selectivity of the signal is affected as well because of its skirt characteristics.

The averaged result of the detected noise power will have a PDF of (16). Therefore, the threshold level having a false alarm rate of P_{FA} can be found by calculating a cumulative density function of (16) and finding the point where it reaches $(1 - P_{FA})$. For example, if the acceptable false alarm rate is 0.1, the threshold level can be calculated, as shown in (24).

$$p_{TH} \approx \mu_N + \frac{6.1265}{\sqrt{N_{AVG}}}(dBm) \tag{24}$$

Figure 27 shows the histogram of the detected noise power over various window frequencies and numbers of average. The wideband white Gaussian noise is generated with a power of -164 dBm/Hz, assuming the system noise figure of 10 dB. MRSS has simulated 200,000 times for each case. Therefore, the case of N_{AVG} = 1 has a total of 200,000 data points, while that of N_{AVG} = 10 has total of 20,000 data points. A window of $\cos^4(\pi f_w t)$ with f_w = 100 kHz has been used with the PLL frequency of 594 MHz. The y-axis shows the

number of occurrences over each 0.3-dB detected power range. The distribution of the detected noise power complies with the log-compressed Rayleigh distribution. To check the validity of (18) and (23), the mean and standard deviation of each result is calculated. By comparing case 1 and 2, the reduction of the standard deviation corresponds well to (18). The shift of the noise floor by 10 dB between case 2 and 3 is due to the ten-time larger f_{NBW} of case 3 than that of case 2.

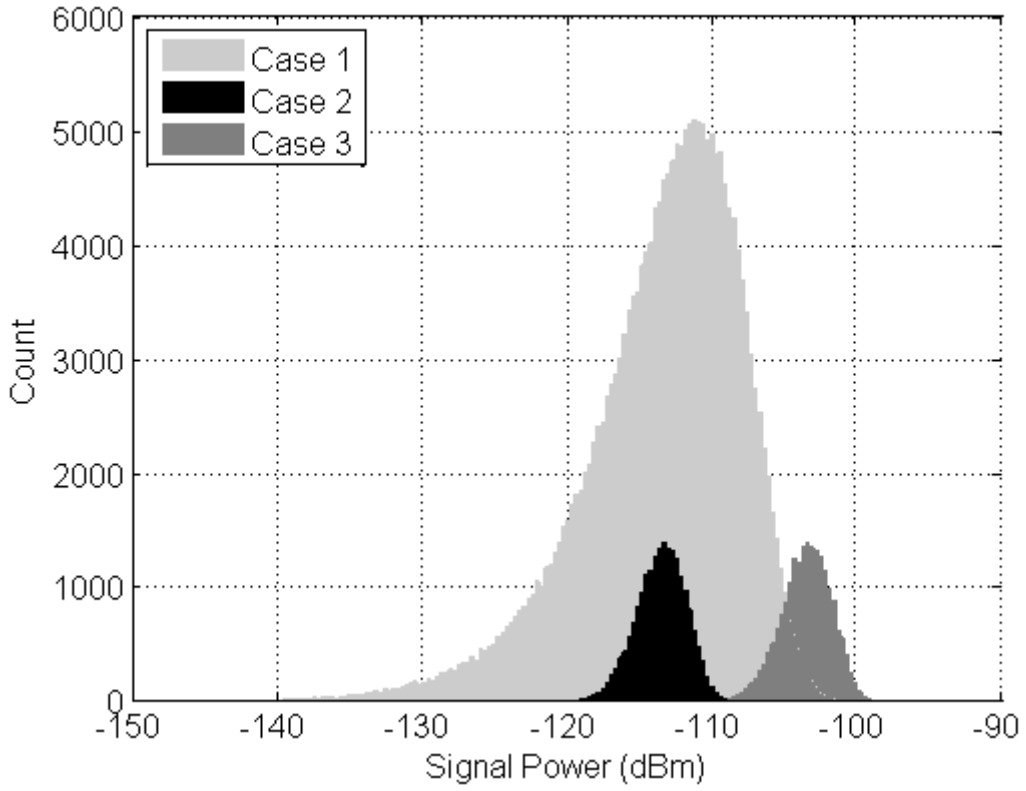


Figure 27. Histogram of MRSS results for noise power measurements with the $\cos^4(\pi f_w t)$ window, (a) Case 1: f_w = 100 kHz, N_{AVG} = 1, (b) Case 2: f_w = 100 kHz, N_{AVG} = 10, (c) Case 3: f_w = 1 MHz, N_{AVG} = 10. The calculated mean and standard deviation are (a) Case 1: μ_N = -113.62 dBm, σ_N = 5.55 dB, (b) Case 2: μ_N = -113.62 dBm, σ_N = 1.74 dB, (c) Case 3: μ_N = -103.63 dBm, σ_N = 1.76 dB.

Figure 28 shows the false alarm rate simulation result when the $\cos^4(\pi f_w t)$ window with f_w = 100 kHz is used. To find the false alarm rate, 200,000 independent MRSS results are gathered and averaged. At each threshold level, the number of averaged results which are larger than the threshold level is counted and normalized with the total number of averaged results, giving the false alarm rate at that threshold. As anticipated by (24), the larger the number of average, the smaller the threshold level which satisfies a certain false alarm rate.

Table 5 compares the theoretical and simulation results on the noise power distribution and threshold level determination. The error is found to be negligible, so the validity of the theoretical model is confirmed.

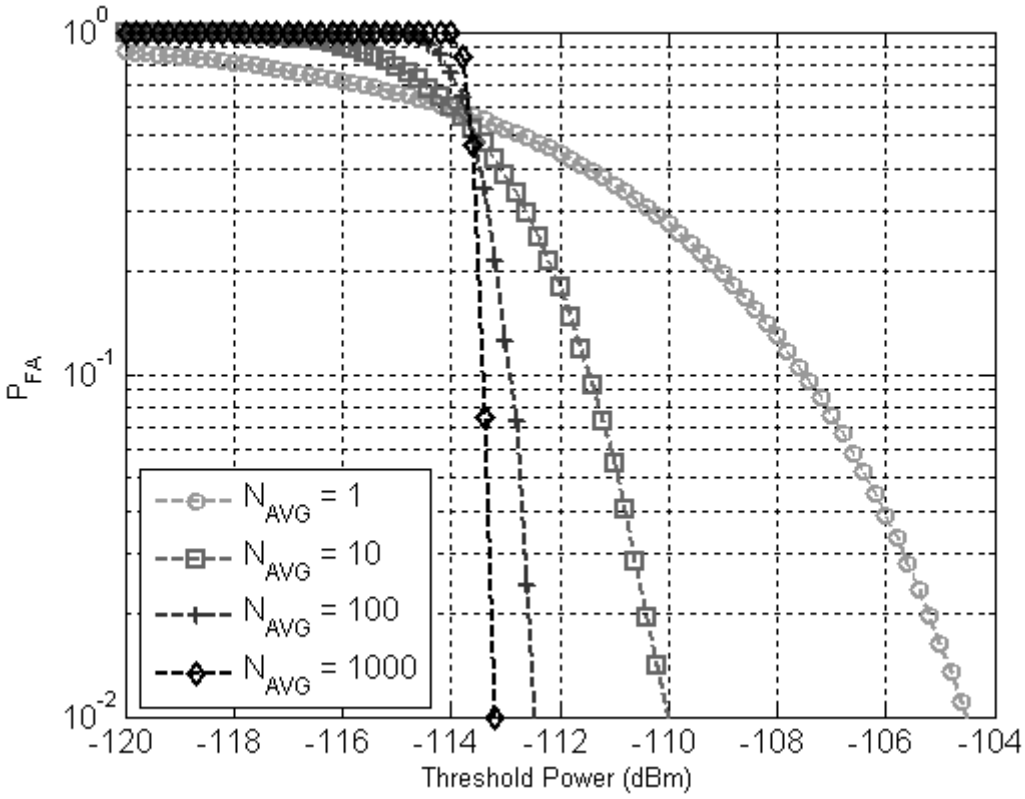


Figure 28. False alarm rate simulation with the $\cos^4(\pi f_w t)$ window of f_w = 100 kHz and various N_{AVG}.

Table 5. Comparison of theoretical and simulation value on the threshold level determination with the $\cos^4(\pi f_\omega t)$ window, f_w = 100 kHz, and P_{FA} = 0.1.

	N_{AVG}	Theoretical Threshold from (20)	Threshold from Simulation	Error (dB)
μ_N (dBm)	All	-113.63	-113.62	-0.01
σ_N (dB)	1	5.57	5.55	-0.02
	10	1.76	1.74	-0.02
	100	0.57	0.54	-0.03
	1000	0.18	0.17	-0.01
P_{TH} (dBm)	1	-107.50	-107.40	0.10
	10	-111.69	-111.40	0.29
	100	-113.02	-112.80	0.22
	1000	-113.44	-113.40	0.04

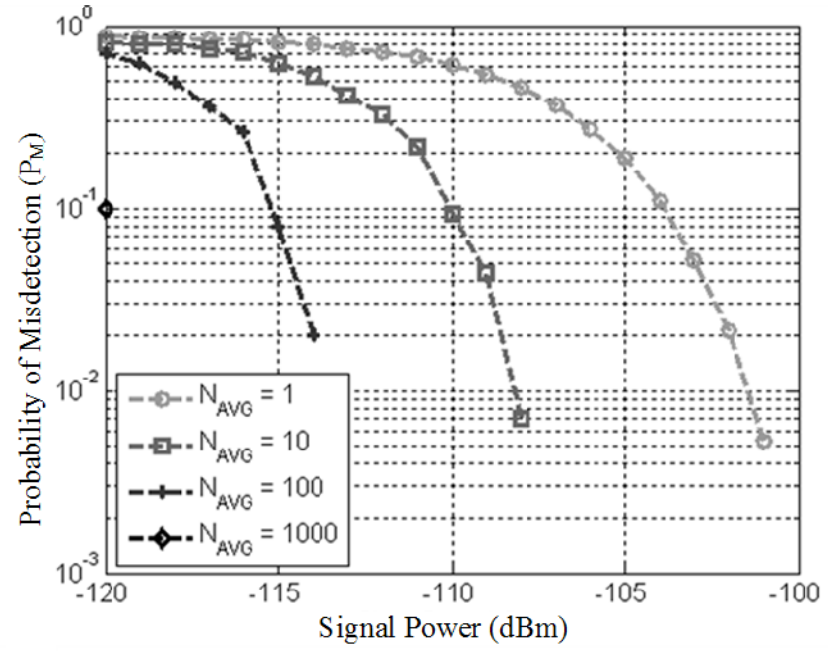
4.2. MRSS Simulation with the Sensing Threshold Level

4.2.1. Probability of Misdetection

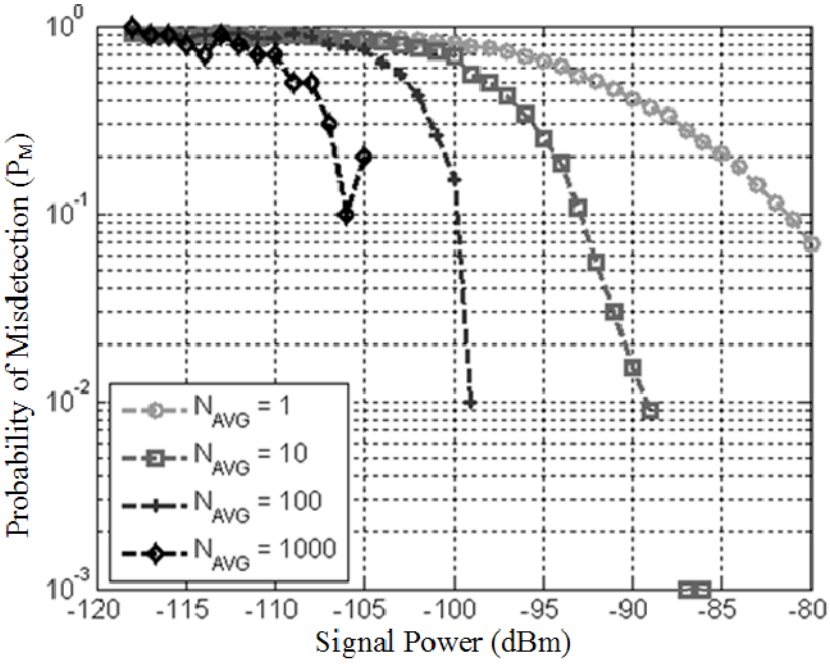
Once the threshold level is determined, the probability of misdetection can be simulated, as shown in Figure 29. In this simulation, the simulated threshold level in Table 5 is used as the sensing threshold level for each N_{AVG}. The window is fixed as a $\cos^4(\pi f_\omega t)$ window with f_w = 100 kHz , and PLL is set to f_c = 600 MHz.

Figure 29(a) shows the case when the input is a continuous wave (CW) signal centered at 600 MHz. The signal power is varied from -120 dBm to -101 dBm. At each signal power, 10,000 independent MRSS results are gathered and averaged with each N_{AVG}. As the number of average is increased, the variance on the detected signal power is also reduced, so the probability of misdetection is also decreased. Figure 29(b) is when the input signal is modulated with 8-level vestigial sideband modulation (8-VSB) according to the ATSC

standard and upconverted to 600 MHz. The signal power shown in the x-axis is the total signal power over the bandwidth of 5.38 MHz [13].



(a)



(b)

Figure 29. Probability of misdetection with the $\cos^4(\pi f_w t)$ window having f_w = 100 kHz with N_{AVG} = 1, 10, 100 and 1000. The input signal is (a) a CW signal at 600 MHz, (b) an ATSC signal at 600 MHz.

Figure 29 tells that with 100 averages, -113 dBm of a CW signal or -99 dBm of ATSC signal within f_{NBW} = 194 kHz can be detected with the probability of misdetection of 0.01. From (6), total processing time would be 1 msec.

The digitally-modulated signals with random data having a symbol rate much faster than the resolution bandwidth of the window can be approximated to have a Gaussian distribution according to the central limit theorem [11]. Therefore, the detected ATSC signal is also subject to the under-response of -2.51 dB with logarithmic processing of MRSS. Thus, the detected signal power with an equivalent noise bandwidth of f_{NBW} in the case of the digitally modulated signal which is fast enough will be

$$\mu_D = p_s - 10\log\left(\frac{f_{BW}}{f_{NBW}}\right) - 2.51 \ (dBm) \tag{25}$$

where μ_D is the detected power, p_s is the original signal power, and f_{BW} is the signal bandwidth. In the case of the ATSC signal with the $\cos^4(\pi f_w t)$ window having f_w = 100 kHz,

$$\mu_D = p_s - 10\log\left(\frac{5.38\times10^6}{1.94\times10^5}\right) - 2.51 \ = p_s - 16.94 \ (dBm). \tag{26}$$

In the case of a CW signal, however, it is represented as a delta function in a frequency domain. Thus, the detected power is not altered by the equivalent noise bandwidth of the window, and the detected power itself is the signal power of a CW signal.

By calculating the average of the data used for Figure 29(b), the average of the detected power of the ATSC signal is within a 1-dB error with the value calculated from (26). This phenomenon can also be found in Figure 23. When f_w is increased by ten times, the detected power of a CW signal is constant, while that of ATSC and DVB-T signals are increased by approximately 10 dB. According to (26), the average detected power will be

-46.94 dBm and -36.94 dBm for f_w = 100 kHz and f_w = 1 MHz, respectively. This is due to the increase of f_{NBW} by ten times in (25).

4.2.2. Phase Noise Effect on the Threshold Level

To downconvert the received RF signal to the baseband, the RF signal should be mixed with a sine or cosine signal from the PLL. When there is no phase noise present at the output of the PLL, the frequency response of the window shown in Figure 20(b) will be the filtering characteristic of MRSS detection. In reality, however, noises from the oscillator's building blocks and external noise make the output of the oscillator noisy and deteriorate the filtering effect of MRSS detection. These unwanted signals are expressed in dB with respect to the carrier signal and referred to as phase noise [14].

Figure 30 shows the effect of phase noise on the MRSS detection characteristics. For this simulation, the $\cos^4(\pi f_\omega t)$ window of f_w = 100 kHz and the PLL frequency of 600 MHz is used. Case 1 is when there is no phase noise applied to the PLL output. Case 2 is when a phase noise of -80 dBc/Hz at 20 kHz, -150 dBc/Hz at 6 MHz and -170 dBc/Hz at 60 MHz offset is applied, and case 3 is when a phase noise of -80 dBc/Hz at 20 kHz, -140 dBc/Hz at 6 MHz and -160 dBc/Hz at 60 MHz offset is used. Once the phase noise is applied, the selectivity of the filter is drastically degraded. A 10-dB increase on the phase noise from case 2 to case 3 results in the 10-dB degradation on the selectivity of the filtering effect of the window. At the 6 MHz offset from the carrier, 594 MHz, the attenuation is about -100 dB and -90 dB for case 2 and 3, respectively. This means that if there is a strong signal at 6 MHz apart from the PLL frequency, that interference signal will be detected with the attenuation of -100 dB for the condition of case 2.

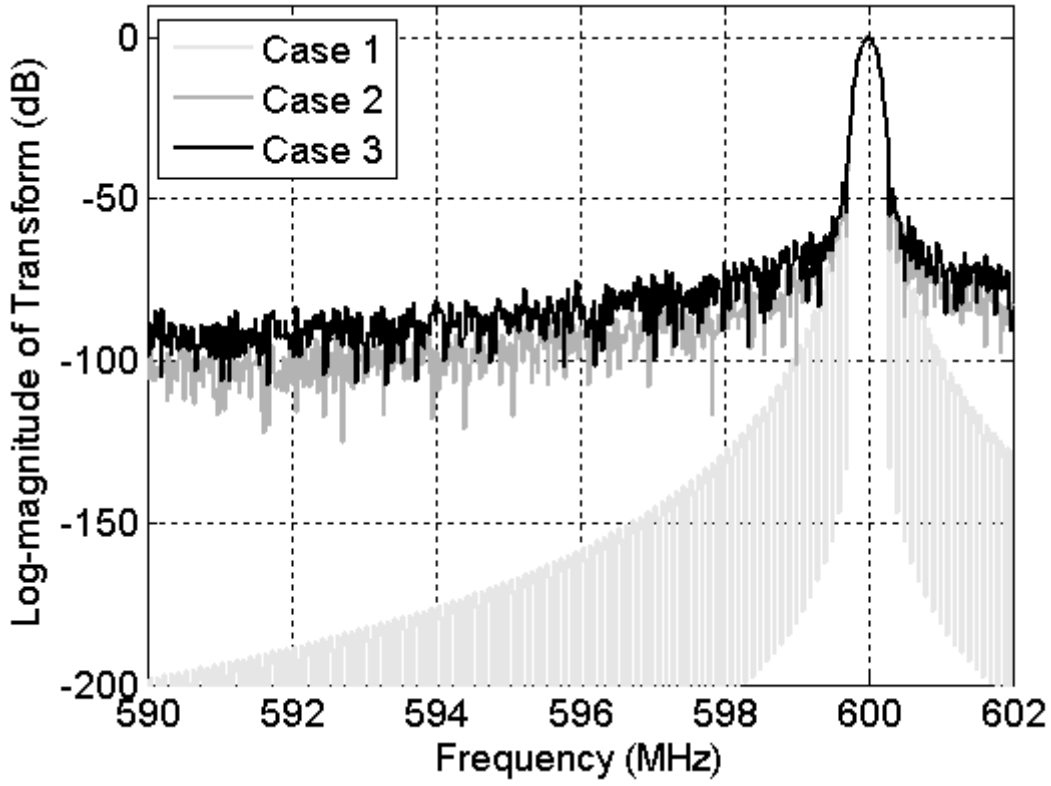


Figure 30. Phase noise effect on the MRSS detection using $\cos^4(\pi f_w t)$ window of f_w = 100 kHz and the PLL frequency of 600 MHz. (a) Case 1: when there is no phase noise, (b) case 2: phase noise of -80 dBc/Hz at 20 kHz offset, -150 dBc/Hz at 6 MHz offset and -170 dBc/Hz at 60 MHz offset, (c) case 3: phase noise of -80 dBc/Hz at 20 kHz offset, -140 dBc/Hz at 6 MHz offset and -160 dBc/Hz at 60 MHz offset.

Figure 31 shows the effect of phase noise on the threshold level with the presence of a strong interference signal nearby. In this simulation, the interference is located at 600 MHz, and the PLL is set to 594 MHz. On each interference power, 10,000 independent results are recorded and averaged by 100 times, and then the threshold level satisfying the false alarm rate of 0.1 is recorded. From Figure 30, when the phase noise of -80 dBc/Hz at 20 kHz, -150 dBc/Hz at 6 MHz, and -170 dBc/Hz at 60 MHz offset is injected, the interference will be detected with approximately -100-dB attenuation. With the knowledge of -113.63 dBm

of noise floor without phase noise injection from Table 3, we can anticipate that the signal having around -13.5 dBm will be reduced by the window to around -113.5 dBm, which is about the same power with the noise floor. When the noise power and the attenuated signal having the equivalent power are combined together, the detected noise floor will be 3-dB above the noise floor without interferer, to be around -110 dBm. From (24), the theoretical threshold level with the average of 100 would be the detected noise floor plus 0.61 dB, about -109.4 dBm. This value matches with Figure 31.

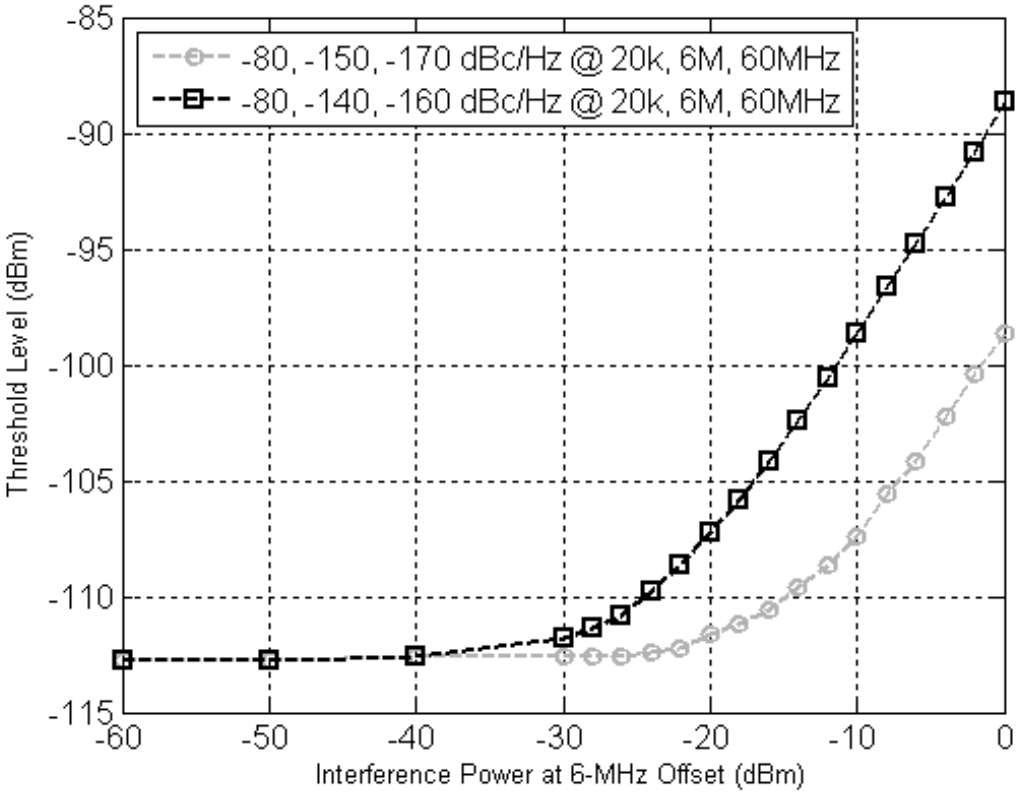


Figure 31. Phase noise effect on the threshold level vs. the interference power located at 6-MHz apart from the PLL frequency when N_{AVG} = 100. The simulation used the $\cos^4(\pi f_w t)$ window of f_w = 100 kHz with injected phase noise of (a) -80 dBc/Hz at 20 kHz offset, -150 dBc/Hz at 6 MHz offset and -170 dBc/Hz at 60 MHz offset and (b) -80 dBc/Hz at 20 kHz offset, -140 dBc/Hz at 6 MHz offset and -160 dBc/Hz at 60 MHz offset.

When the interference power is below the noise floor plus the attenuation, the effect of interference is negligible within the error of 3 dB. The phase noise reduction of 10 dB results in the 10-dB increase of the allowable interference power with the same threshold level degradation. Therefore, once the desired system specification on the maximum signal power and the minimum sensing threshold is determined, the requirement on the phase noise of the PLL can be decided.

4.3. Summary

The statistical distribution model on the detected noise power by the MRSS technique is derived. Based on this model, a simple way of deciding the sensing threshold level is investigated and verified with the simulation. The threshold level can be lowered when the system noise figure is decreased, when the window has a low equivalent noise bandwidth, f_{NBW}, or when the number of average, N_{AVG}, is increased. Upon the threshold level decision, the spectrum sensing capability has been shown on various signal types. With 1 msec of observation time, -113 dBm of a CW signal or -99 dBm of the ATSC signal within 194 kHz of the detection bandwidth can be sensed with the probability of misdetection of 0.01. Furthermore, the effects of undesired phase noise of the local oscillator on the threshold level are presented and analyzed with the presence of the strong interferer. With the 3-dB margin in the threshold level, MRSS can tolerate up to -13.5 dBm of a CW signal at the 6-MHz offset when the phase noise of the oscillator is -80 dBc/Hz at 20 kHz, -150 dBc/Hz at 6 MHz, and -170 dBc/Hz at 60 MHz offset.

CHAPTER 5

FULLY INTEGRATED MRSS RECEIVER

5.1. Architecture

Figure 32 shows a block diagram of the fully integrated MRSS receiver, which operates either as a spectrum sensing block or as a receiver front-end block. The main feature of the proposed architecture is to maximally share the RF front-end such as the low-noise amplifier (LNA) and a mixer in a receiver path so the receiver can be switched between the receiver mode and MRSS mode through control of the integrated serial bus interface.

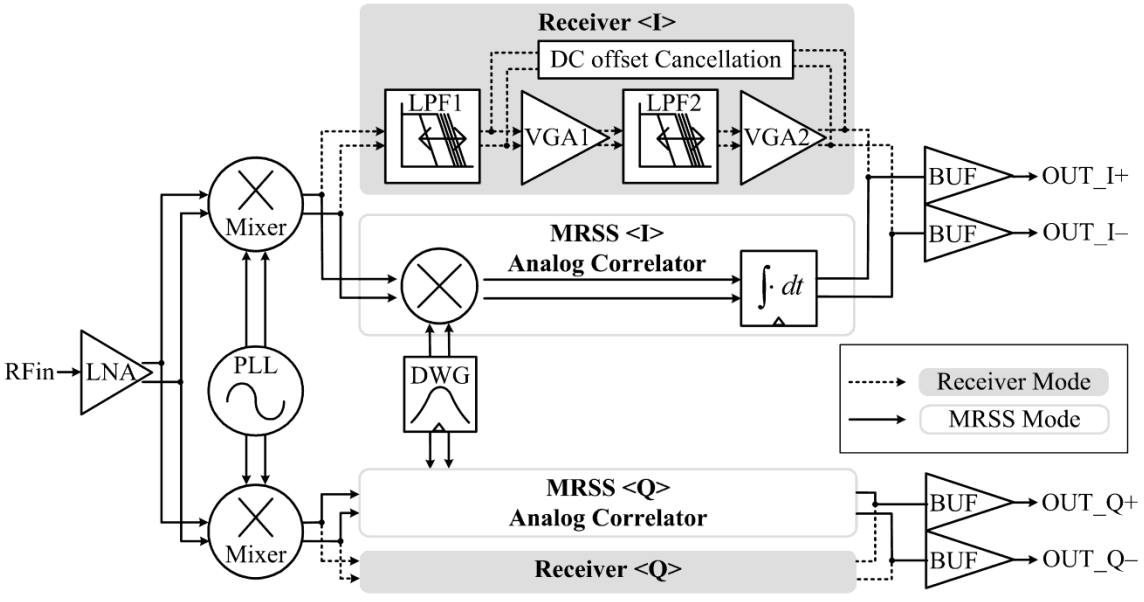


Figure 32. A block diagram of the fully integrated MRSS receiver.

In the receiver mode, the MRSS receiver is configured as a direct-conversion receiver. The RF input signal is amplified through the LNA and downconverted to baseband by a

passive mixer. The baseband filter consists of a second-order LPF, a variable-gain amplifier (VGA), sixth-order LPF, and a VGA with a dc-offset cancellation block. The PLL is a third order, 20-bit fractional-N type. The simulation shows that the total noise figure of the RF front-end is 4 dB with a gain of 25 dB and an input-referred 1-dB gain compression point (P_{1dB}) of -27 dBm. In this mode, most of the MRSS blocks are disabled to reduce the power consumption.

In the MRSS mode, the MRSS receiver is configured as a spectrum sensing energy detector. The downconverted baseband signal is correlated with a window generated from the DWG, yielding the filtered output within the window bandwidth. The outputs in the I and Q paths are digitized by the external ADC, and the signal power is computed by $(OUT\_I^2 + OUT\_Q^2)^{0.5}$. In this mode, no analog filter is used in the RF signal path. The filtering effect comes from correlating the baseband received signal with a window. In this mode, all baseband filter blocks are disabled to save the power consumption.

5.2. Key Building Blocks

5.2.1. Digital Window Generator

The digital window generator (DWG) generates a window waveform with flexible durations. It is composed of a static RAM (SRAM), a DAC, and an LPF, as shown in Figure 33.

The SRAM is configured as four banks of 224×11b. One bank of RAM stores one window data with the margin of N_{buf}, typically 32, at the end of RAM so it can store four different types of windows at one time. The DAC has 11-bit resolution using R-2R ladders, and the LPF is sixth-order Chebyshev type II. Changing the RAM address from 0 to 223

generates window raw data for the DAC. The LPF reconstructs the digital window signal to an analog form by removing the harmonics of the clock frequencies from the DAC. The frequency and the harmonics of the clock are known in advance, and the bandwidth of the window signal in RAM is much less than the clock frequency. Moreover, the LPF can more easily meet the requirement for noise and linearity than an LPF in the receiver path. So, we can implement the LPF with the low power and small area.

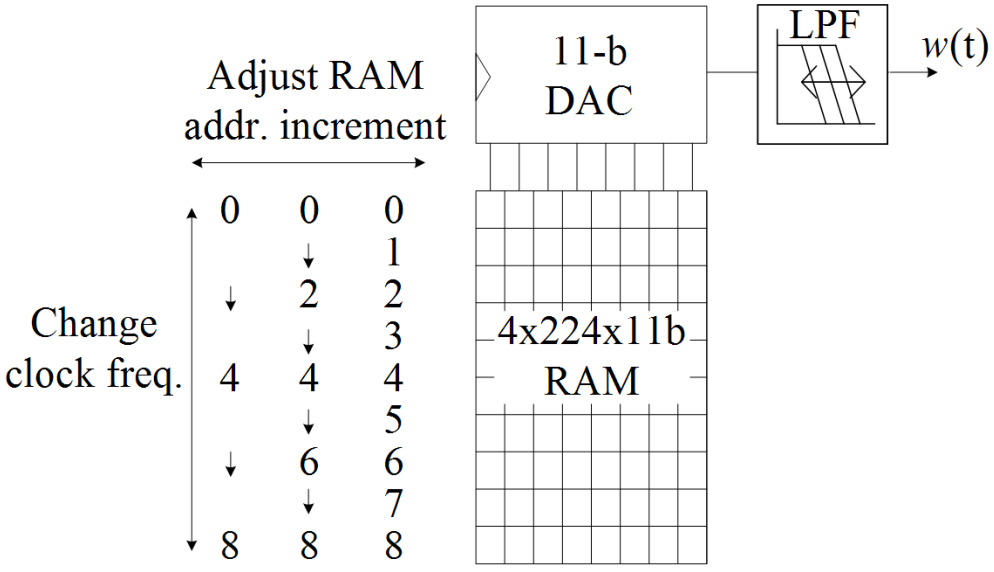


Figure 33. The architecture of the digital window generator.

The window duration, t_{ω}, can be changed by two methods: by changing the clock frequency, f_{clk}, or by adjusting the RAM address increments, N_{inc}. The clock frequency can be controlled by setting the divider connected to the 38.4-MHz external crystal oscillator to a ratio value N_{div}, i.e., one, two, four, or eight. If more flexibility is required, the internal divider can be disabled and an external arbitrary clock, f_{clk_ext}, can be used. In summary, the window duration can be obtained by (27).

$$t_{\omega} = \frac{224 - N_{buf}}{f_{clk} N_{inc}} (\text{sec}) \text{ where } f_{clk}(\text{Hz}) = \begin{cases} f_{clk\_ref} / N_{div}, & \text{if CLK\_EXT} = 0 \\ f_{clk\_ext}, & \text{if CLK\_EXT} = 1 \end{cases} \quad (27)$$

Figure 34 depicts the conceptual timing diagram of DWG operation. Figure 34(a) shows the longest window generation, with the slowest clock frequency and an address increment of one. Figure 34(b) shows a window that is twice as fast by only changing the address increment to two with the same clock frequency. Figure 34(c) also shows window generation that is twice as fast as that of Figure 34(a) by doubling the clock frequency and maintaining the address increment as one. Therefore, by combining the clock frequency and address increment control, the window duration can be further changed; thus the detection bandwidth of the MRSS can be adjusted. Figure 35 presents the measurement results of $\cos^4(\pi f_{\omega} t)$ windows from the DWG with variations of the address increment and the clock frequency.

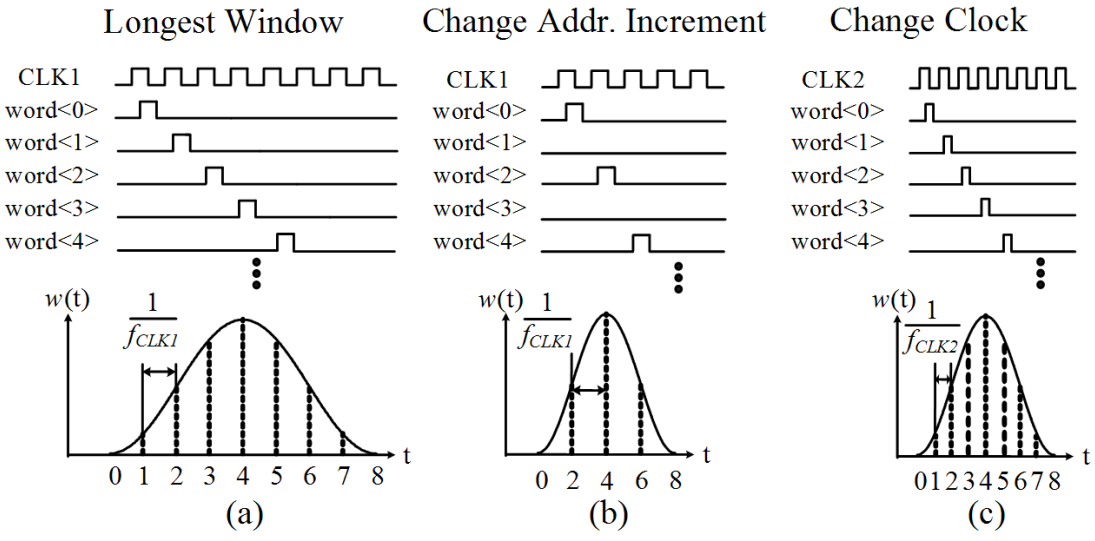


Figure 34. DWG output examples showing a timing diagram for (a) the longest window, (b) twice faster window by changing the address increment, and (c) twice faster window by changing the clock frequency.

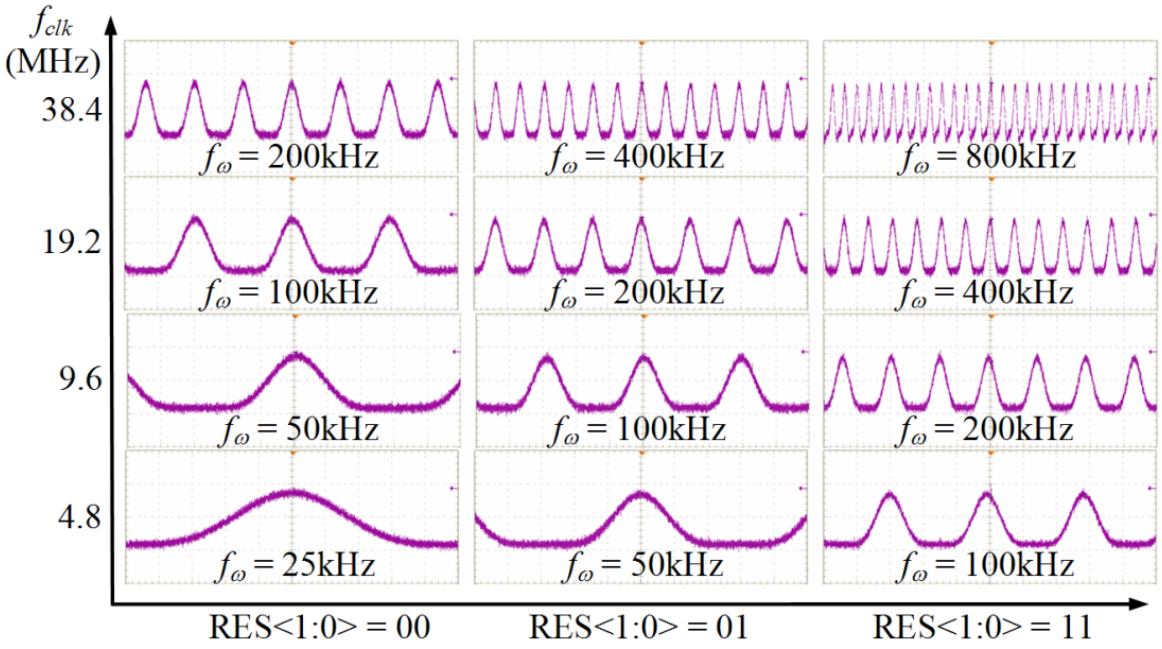
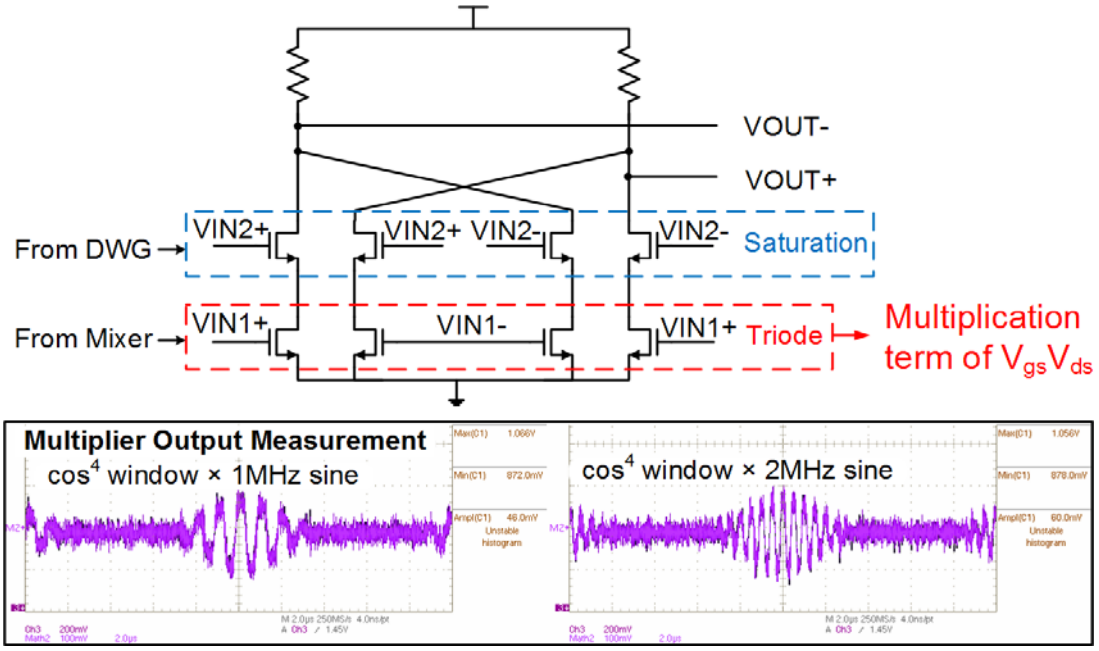


Figure 35. DWG output measurement results with variations of the address increment and the clock frequency.

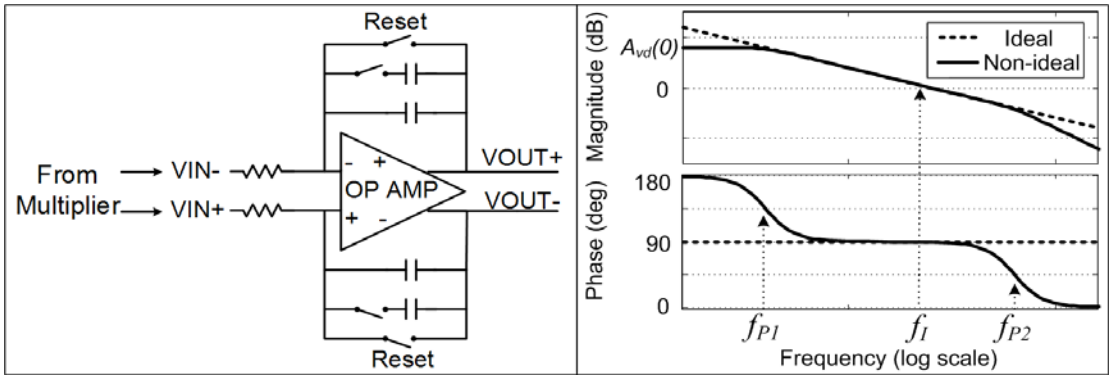
5.2.2. Analog Correlator

To correlate the baseband signal from the mixer with the window generated from the DWG, those two signals are multiplied and integrated. Figure 36(a) shows a simplified schematic of the analog correlator consisting of a multiplier and an integrator. In the multiplier, the four upper transistors are source followers, thereby transferring the input signal to the drain of the bottom transistors. The four bottom transistors are biased in the triode region to produce the multiplication term of $V_{gs} \times V_{ds}$ [24]. The multiplier output is integrated during the window duration. The AC response of the ideal integrator has a pole at DC and has a constant phase of 90°. However, the non-ideal nature of the op amp results in a pole above DC. A correlator simulation showed that this dominant pole should be less than 1/5 the window frequency, f_ω, to prevent the leakage of signal detection [25]. The

feedback capacitor value can be programmed to adjust this non-ideal pole position and the gain of the integrator. An internal timing block in the DWG generates a reset signal after each correlation to initialize the integrator. Figure 36(b) shows the measured multiplier output of the multiplication of the window signal from the DWG and the downconverted continuous wave (CW) at 1 MHz and 2 MHz, respectively.



(a)



(b)

Figure 36. (a) The architecture of the analog correlator and (b) the multiplier output measurement.

Figure 37 is a time-domain snapshot of the MRSS measurement, showing three consecutive MRSS operations. The first line is a 400-kHz $\cos^4$ window from the DWG. The RF input is a -50-dBm CW signal at 600 MHz, and the PLL is set to 600.2 MHz. Therefore, the downconverted baseband signal is 200-kHz CW. Because the baseband signal is within the detection bandwidth of the window, the output of the analog correlator is high. A reset signal is shown as a reference.

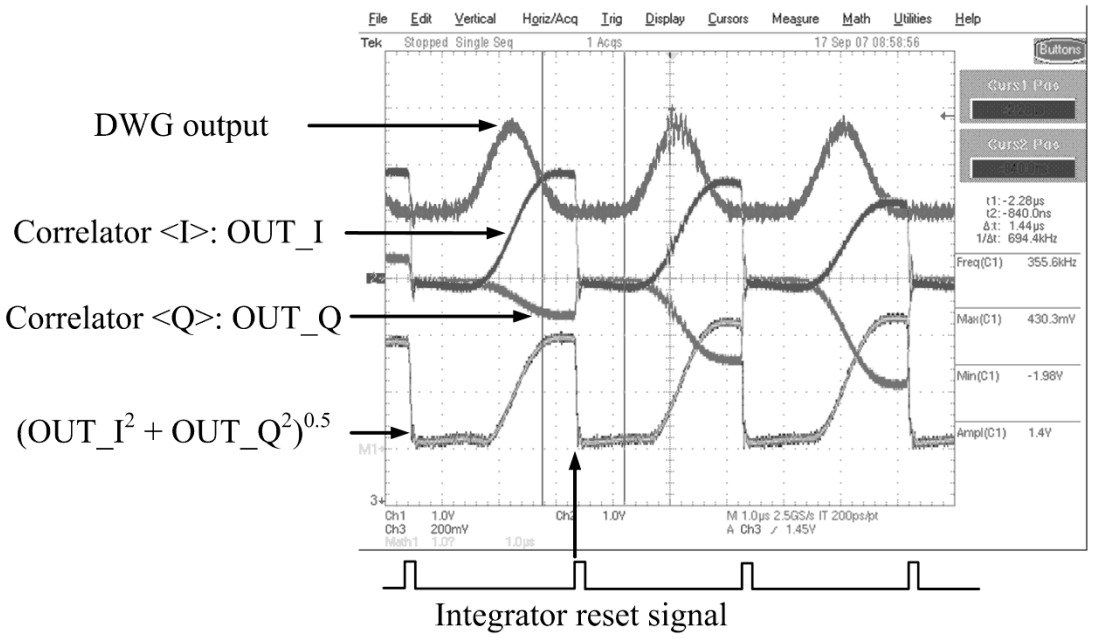


Figure 37. A snapshot of the MRSS time-domain measurement.

5.3. Experimental Results

5.3.1. Measurement Setup using CR Testbed

The MRSS receiver has been fabricated using 0.18-μm CMOS technology. The fabricated IC microphotograph is shown in Figure 38. RF blocks such as the LNA, mixer,

LC voltage-controlled oscillator (VCO), and PLL are used in both the receiver and MRSS modes. Baseband filters and MRSS blocks are switched, depending on the operation mode. The overall die occupies 4.8 mm × 2.4 mm.

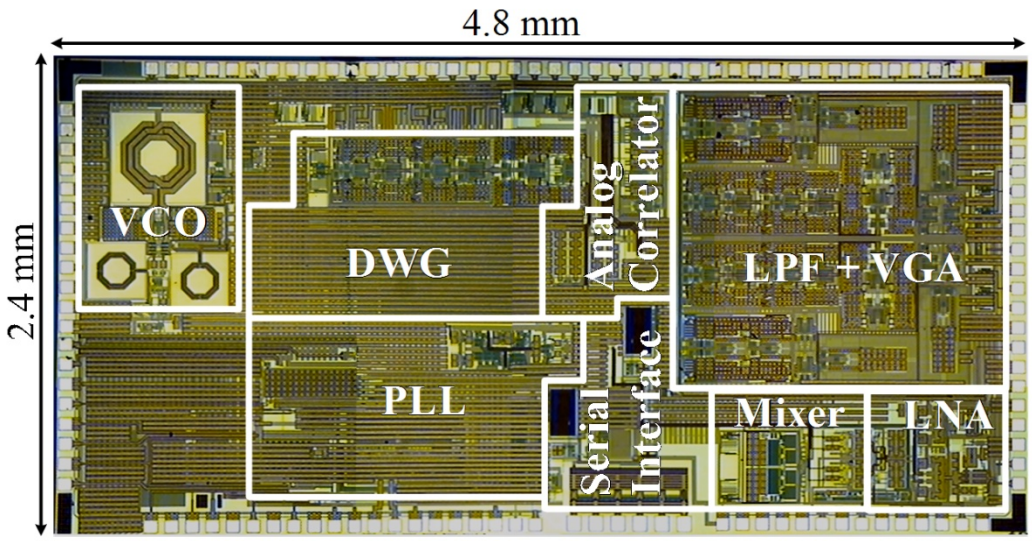


Figure 38. Die microphotograph.

Figure 39 shows the measurement configuration and its photograph for the test of the fabricated MRSS receiver using a fully automated CR testbed. A multi-standard, fully software-driven testbed system has been developed to support thorough characterization of its own CR system and IC designs [26]. This system has a capability of instant testing and evaluation of the communication system and RF/analog ICs and modules. The performance of the receiver can be evaluated by comparing the test board with the spectrum analyzer, which is an ideal energy detector. The fabricated IC is mounted on the test board with wire-bonding interconnection. Because the gain of the LNA, mixer, and the analog correlator vary with temperature and process, the system needs to be calibrated to

measure the absolute power. Before doing the measurement, one-point calibration is performed with a -50-dBm CW signal.

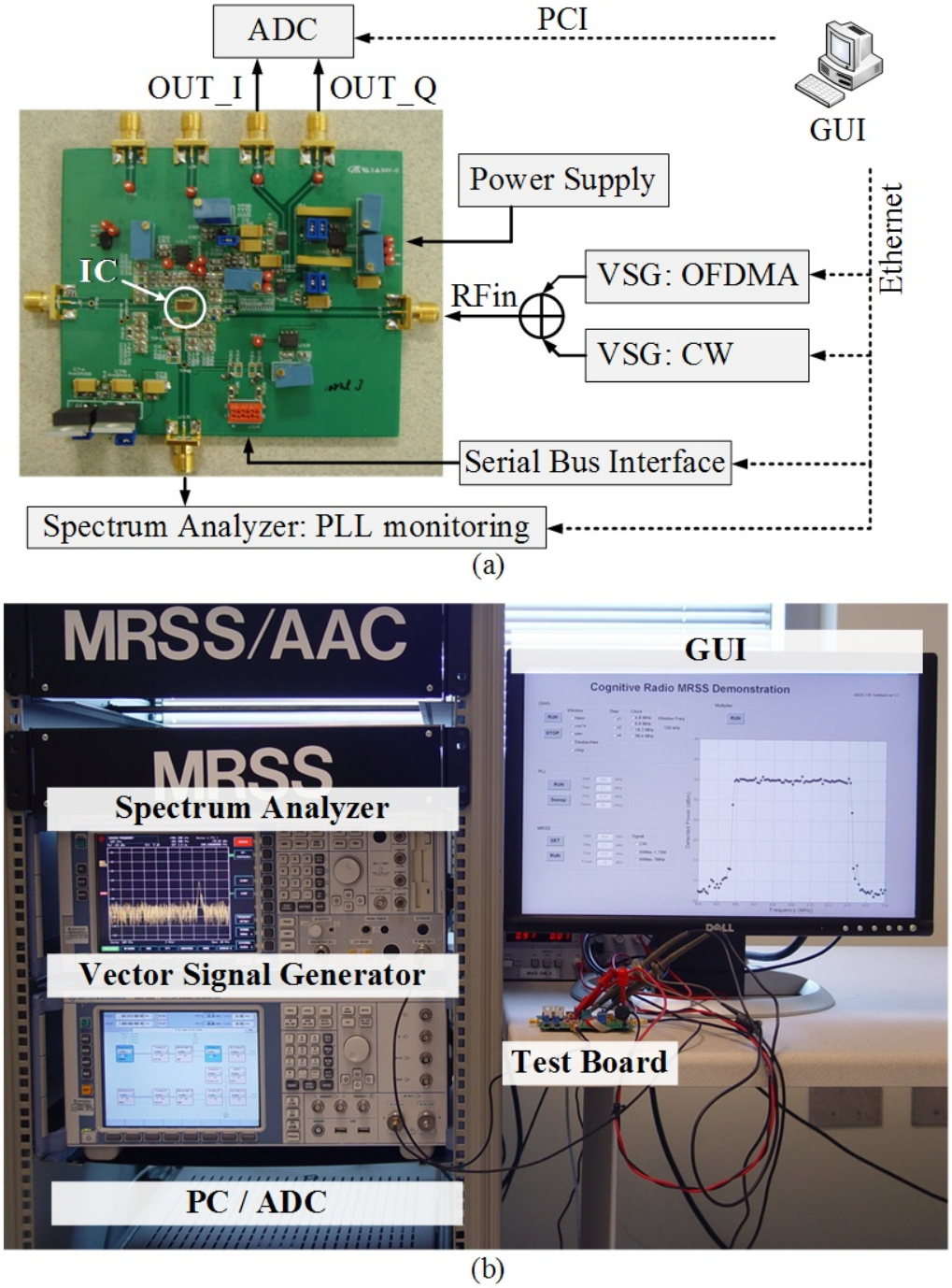


Figure 39. Fully automated CR testbed, (a) its configuration diagram and (b) a photograph.

5.3.2. MRSS Measurement

In-band energy detection performance has been measured, as shown in Figure 40, with a CW input and 100-kHz $\cos^4$ window by changing the input power and observing the detected power. The frequency of the RF input signal and PLL is set to 603 MHz. The ideal response is a straight line with a slope of 1 dB/dB, so the detection error can be calculated by the deviation from the ideal response. Within ±1-dB error from the ideal response, MRSS has a detection dynamic range of 32 dB from -74 dBm to -42 dBm. Below -74 dBm of the input power, the detected power is too close to the noise level, and above -42 dBm of the input power, the correlator circuit starts to saturate. Since our idea is to create a filtering effect with arbitrary resolution by multiplying window signals, it is expected that sensitivity would be worse than that of the receiver with physical filters. Considering the noise figure and the bandwidth of the system and the signal-to-noise ratio (SNR) margin, however, there is room for improvement in detection sensitivity.

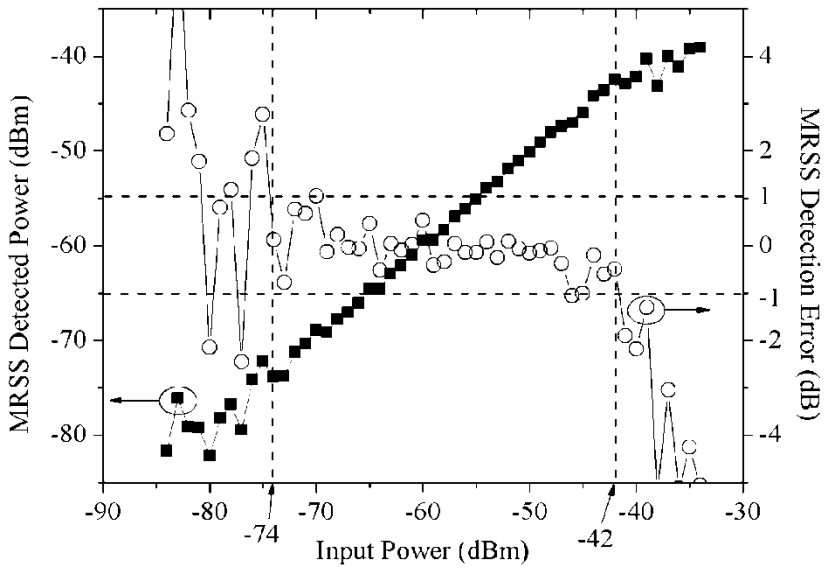


Figure 40. MRSS in-band detection with 100-kHz window.

Figure 41 shows the measured window filtering characteristics, in-band detection and out-of-band rejection performance. A CW signal of -42 dBm at 603 MHz has been detected with 100-kHz $\cos^4$ window and 400-kHz $\cos^4$ window, respectively. The PLL has been swept from 600 MHz to 606 MHz with a frequency step of 50 kHz and 100 kHz for 100-kHz window and 400-kHz window, respectively. Because of the filtering effect of windows, the signal is detected only when the downconverted signal is within the detection bandwidth of the window. As stated previously, a short window has a wide detection bandwidth, and a long window has a narrow detection bandwidth. Therefore, flexible detection bandwidth control is achieved by digitally changing the DWG settings without using any filter banks. Lower noise floor and narrower bandwidth are achieved with a longer window at the expense of longer detection time, as shown in (6).

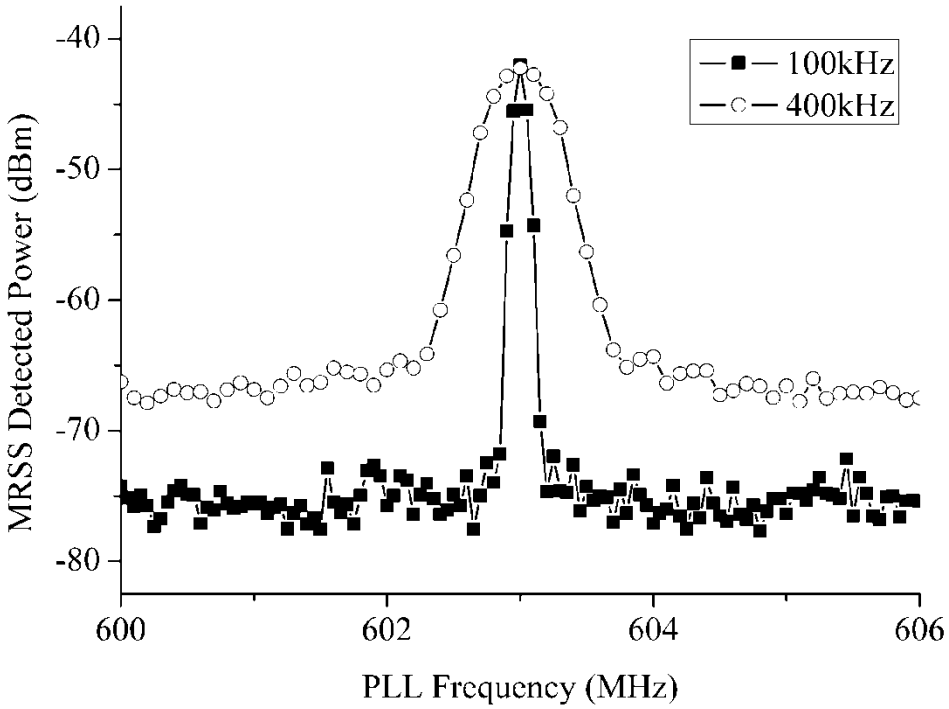


Figure 41. MRSS detection bandwidth control with 100-kHz and 400-kHz windows.

Figure 42 shows the interference rejection characteristic with a 100-kHz $\cos^4$ window by changing the input signal power at various frequency offsets from the PLL frequency. The input is a CW signal fixed at 603 MHz, and the PLL has been changed to 603, 603.5, 606, and 612 MHz, respectively. The first case without any offset is when the signal is within the detection bandwidth. The other cases are when the signal is out of the detection bandwidth, so it should not be detected. The measurement shows about 35-dB rejection for the interferer without using any filter in the RF signal path.

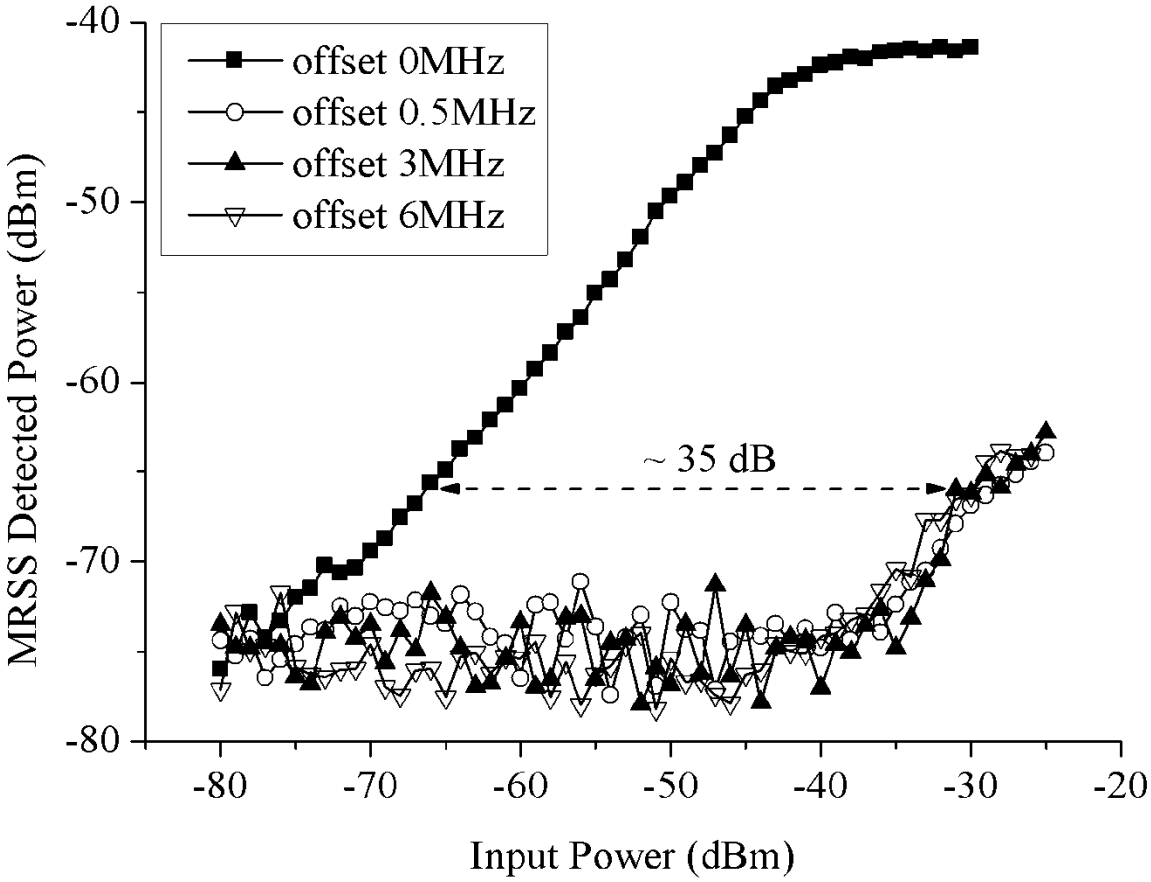


Figure 42. Measured MRSS interference rejection characteristic.

In addition to detecting CW signals, MRSS can detect any kind of complex modulated signals. Figure 43 compares the MRSS response with that of a spectrum analyzer. An OFDMA-modulated signal with the 7-MHz bandwidth and the -35-dBm channel power centered at 609 MHz was combined with a -50-dBm CW signal at 603 MHz and applied to the spectrum analyzer and the MRSS receiver, respectively. Figure 43(a) is the output spectrum from the spectrum analyzer with the resolution and video bandwidth of 200 kHz. Figure 43(b) shows the average of 100 independent MRSS measured results using a 100-kHz $\cos^4$ window, having a theoretical equivalent noise bandwidth of 194 kHz. MRSS is detecting a signal power within its equivalent noise bandwidth, so an OFDMA signal with -35 dBm of the channel power and the 7-MHz bandwidth is detected at about a -50-dBm power level, which is the same as in the spectrum analyzer. Therefore, it shows that MRSS can detect the RMS power of an arbitrary signal within its detection bandwidth, working as a simple spectrum analyzer.

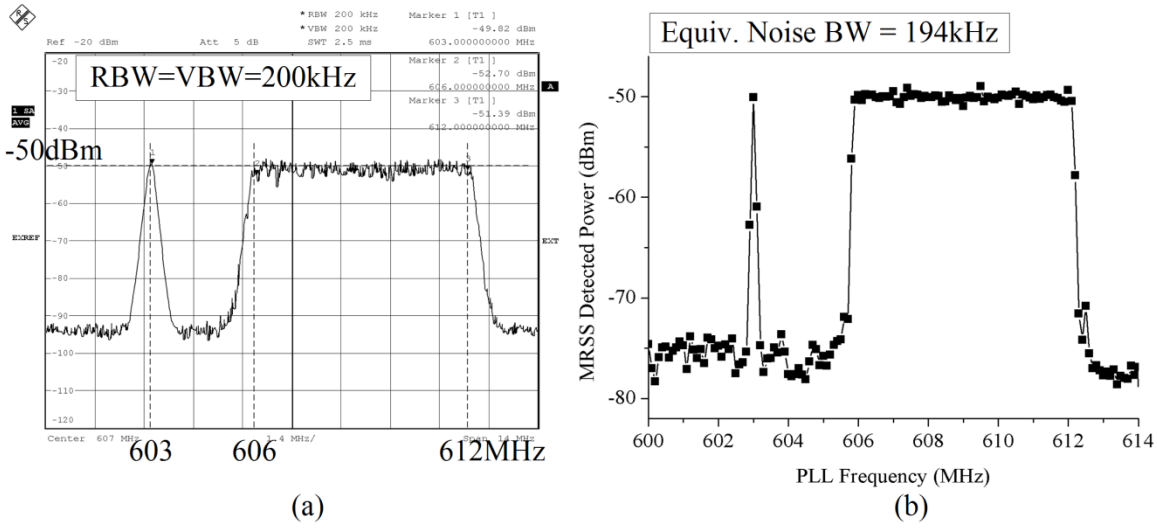


Figure 43. Comparison of a spectrum analyzer and the MRSS response.

Figure 44 shows the effect of averaging on the same detection environment as in Figure 44(b) with the averaging number, N_{AVG}, of 1, 4, 16, and 64, respectively. Unlike the CW signal, which has almost the constant power at all times, the instantaneous power of white Gaussian noise and a Gaussian-like OFDMA signal has large variation over time. Therefore, it is desirable to have a certain level of averaging to minimize its variation [27]. As the number of samples averaged is increased, the variations become small, but this improvement comes at the expense of longer detection time, as shown in (6).

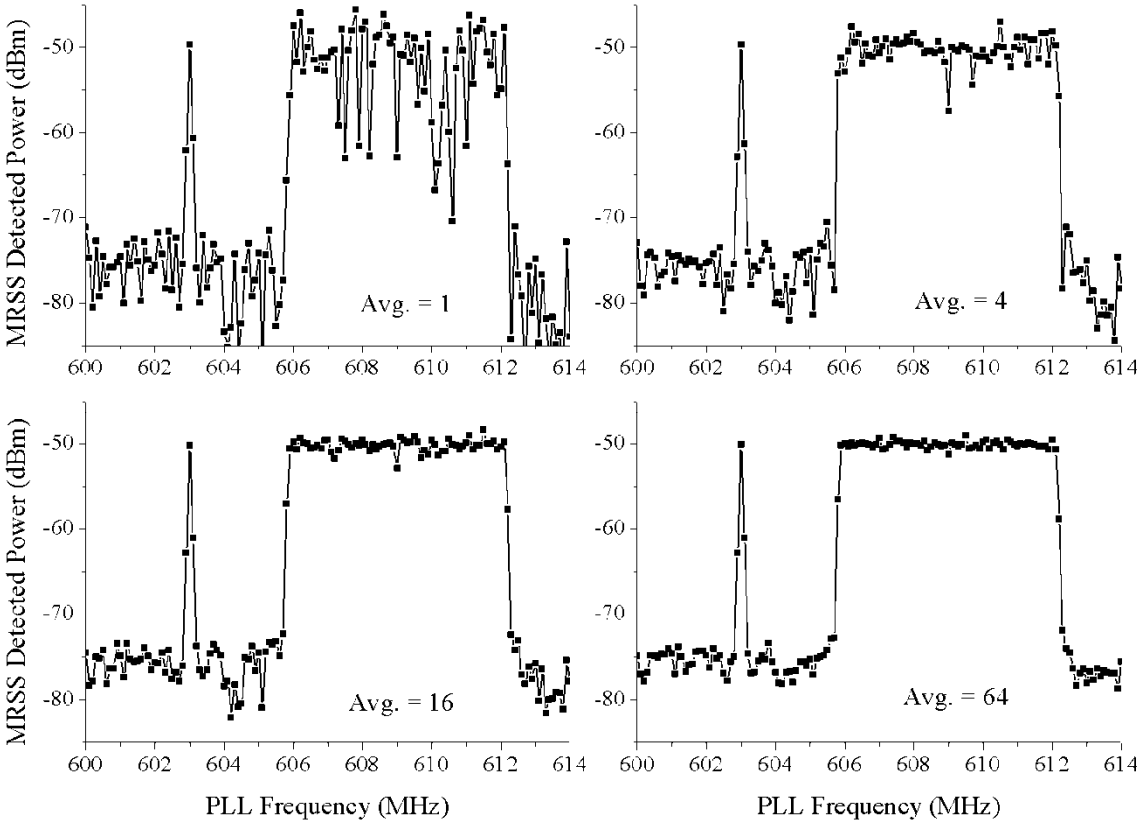


Figure 44. Averaging effect on MRSS detection with various averaging numbers.

Table 6 shows the power breakdown of the MRSS receiver. It consumes about 180 mW for both the receiver and MRSS modes with a 1.8-V supply voltage.

Table 6. Power breakdown of the MRSS receiver.

Blocks		MRSS mode (mA)	Receiver mode (mA)
RF	LNA & Mixer	17	17
	VCO & PLL	34	34
Baseband	LPF & VGA	0	18
MRSS	Analog correlator	8	0
	DWG	16	3
Etc		25	25
Total		100	97

5.4. Summary

A fully integrated UHF receiver with MRSS spectrum sensing functionality has been designed and fabricated using a 0.18-μm CMOS technology. The MRSS receiver works as a simple spectrum analyzer with low complexity and power consumption thanks to the proposed digitally assisted analog signal processing technology. The detection time and sensing threshold can be controlled by selecting an appropriate windowing signal. When a 100-kHz $\cos^4$ window is used, detectable sensitivity of -74 dBm with a 32-dB dynamic range was obtained. The MRSS receiver has a scalable architecture in terms of area and power consumption as it is possible to be easily migrated into deep sub-micron technology. The MRSS functionality can be adopted in an RF front-end for spectrum sensing of future CR wireless communication systems.

CHAPTER 6

SPECTRUM FILTERING TECHNIQUE

6.1. Motivation

Cognitive radio (CR) technology aims to increase the efficiency of spectrum utilization by opportunistically using a vacant channel. While the spectrum sensing technology is necessary to start the CR communication, spectrum filtering technology is essential to maximize its throughput of CR systems. Because there is no guarantee on the availability of enough spectrum segments for every CR users, even a small fraction of spectrum segments should be fully utilized through channel bonding or channel splitting technique. Moreover, the harmful effect of interference between the primary users and the CR users should also be minimized with proper filtering techniques. Therefore, adaptive configuration of the bandwidth and the type of the baseband filter is an essential functionality for the CR system. One of the key enabling technologies of variable bandwidth communication is a tunable baseband filter which can change its bandwidth, type and order as needed.

6.2. Conventional Baseband Filtering Methods

So far, various tunable filtering methods have been proposed, which can be categorized into the digital control method [28], [29] and the analog tuning method [30].

The digital control method is to use component array banks in binary or thermometer arrangement. To make a bank, multiple resistors, capacitors, or transconductors are placed

in series or in parallel so the combined bank can have a desired value. Figure 45 shows an example of making a tunable capacitor with a binary code and with a thermometer code. The digital control method is popular with its simplicity, but the element tends to become larger if high tunability is required, and the control resolution is limited to the minimum unit component value. Therefore, higher tunability comes with more complexity and larger die area.

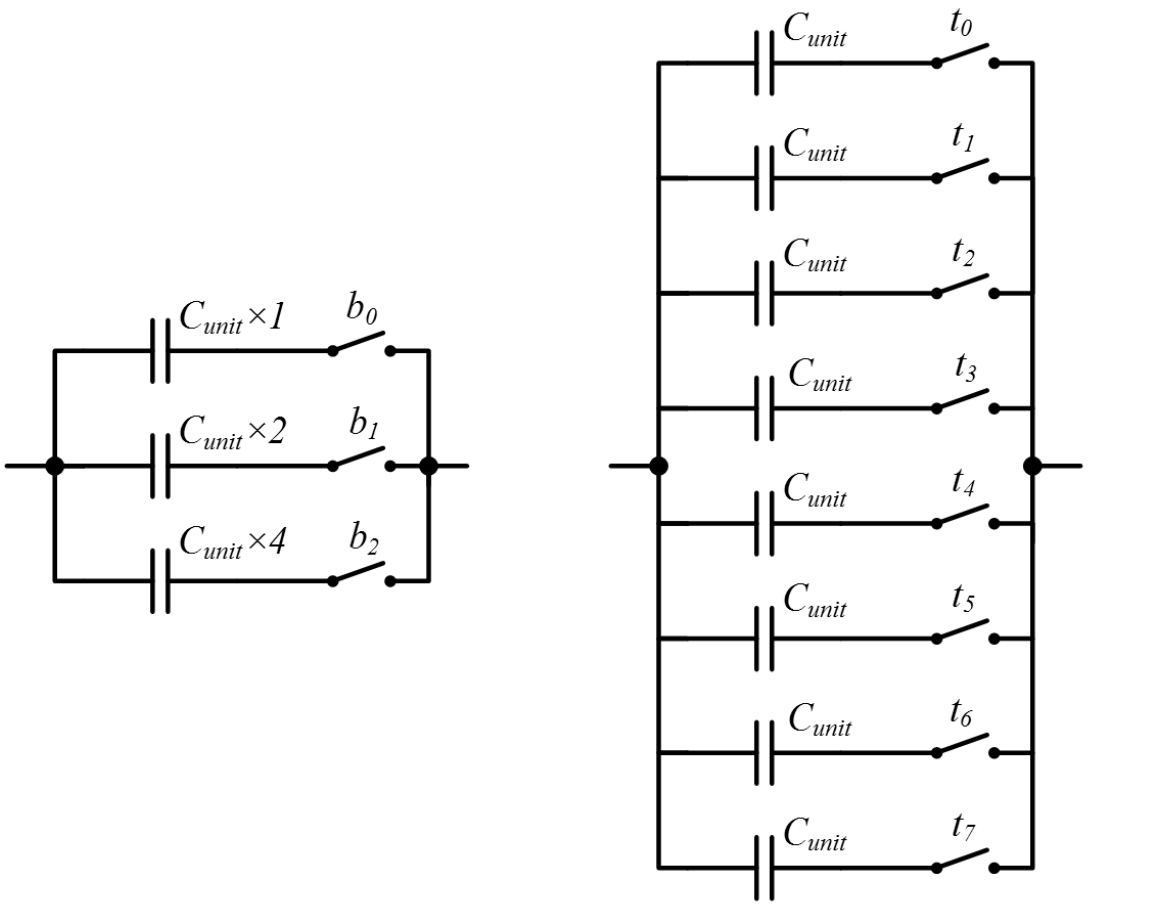


Figure 45. Examples of a digital control method: control of capacitance (a) with a binary code, and (b) with a thermometer code.

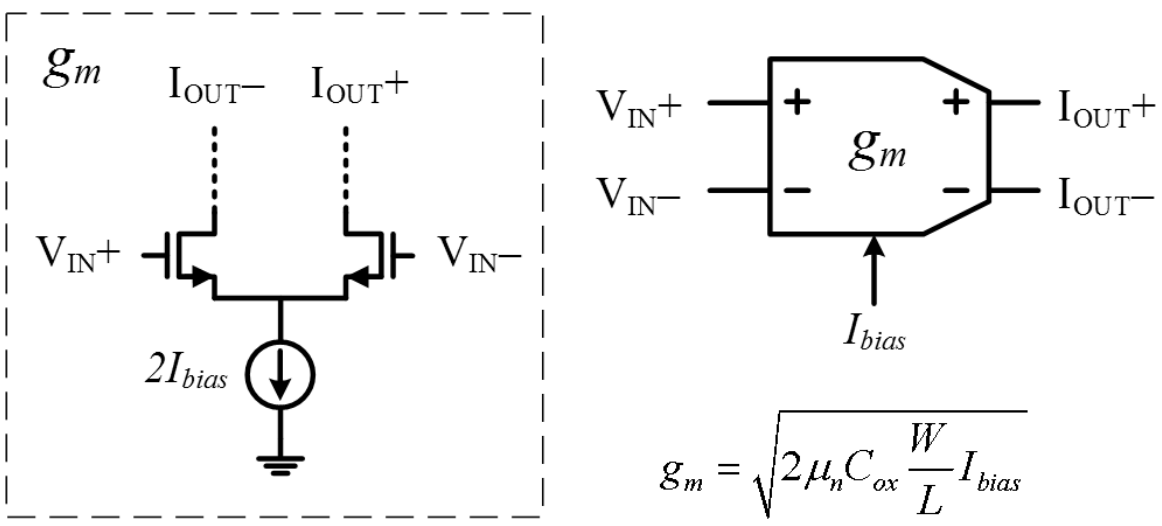


Figure 46. Example of an analog tuning method: control of transconductance by changing the bias current, I_{bias}.

The analog tuning method is to adjust component value in an analogous way. The variables for the adjustment can be resistance, capacitance, inductance, or transconductance. Figure 46 shows control of transconductance by changing the bias current. As long as the device is in saturation, the transconductance of the device is approximately proportional to the square-root of the bias current. Therefore, the transconductance of the device can be controlled by adjusting its bias current. Although this method can be implemented in a simple way, it is hard to achieve a precise resolution because of the PVT variations.

Recently, a tunable G_m-C filter has been published that uses a pulse-width modulation (PWM) generator to adjust the effective transconductance [30]. Figure 47 shows the conceptual diagram of achieving the effective transconductance by changing the duty ratio of PWM signals. By adjusting the effective G_m without explicitly changing hardware

connections, it can be highly programmable with a limited number of components. However, its tuning resolution is limited by the accuracy of the PWM signal, which is 1/32 at its maximum bandwidth in case of [30] due to the accuracy of the duty-cycle control PWM signal.

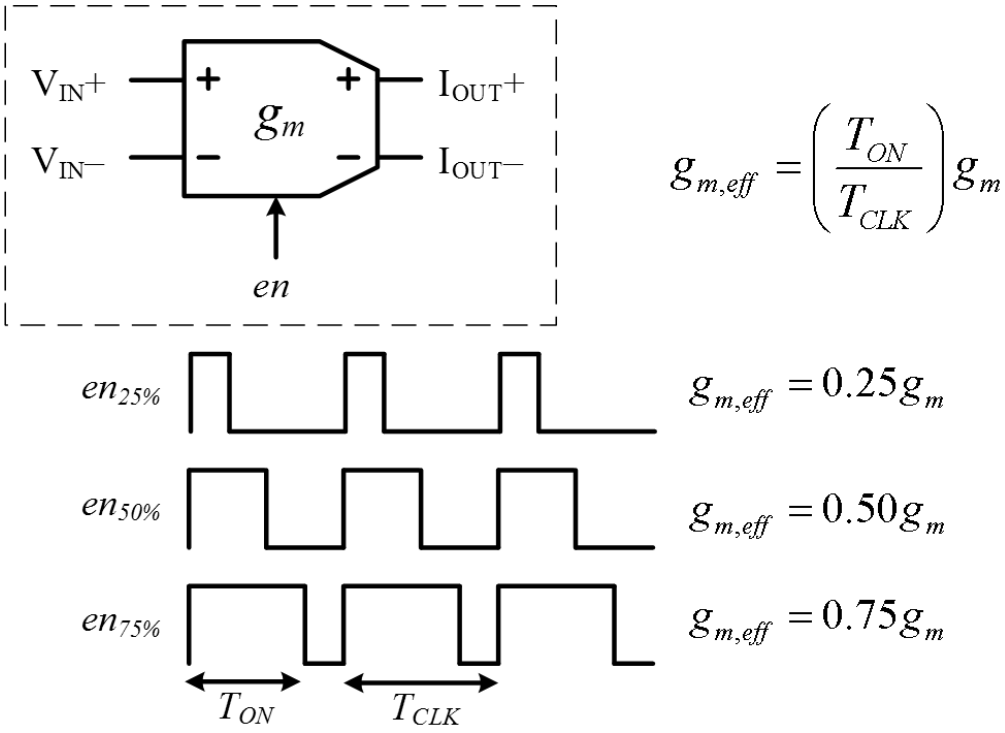


Figure 47. Fractional transconductance control by using PWM signals.

6.3. Proposed Reconfigurable CMOS Analog Baseband Filter

In the proposed architecture, the bandwidth and the type of a filter can be digitally configured by changing the transconductance of G_m cells using ΔΣ modulators (ΔΣMs). The adoption of ΔΣ modulation for high-speed dithering of the unit G_m cell increases the controllability without using excessive number of unit cells [31]. Compared with the

conventional approaches using a component bank [28], [29], the number of unit cells for the same resolution can be significantly reduced. Also, compared with the PWM control method, the proposed architecture has a higher control resolution for the same clock frequency because of the noise shaping property of the ΔΣMs. The bandwidth control resolution is measured to be less than 30 kHz owing to fractional ΔΣM control. Such high tuning resolution promises the possibility of using such control scheme not only for the reconfiguration but also for the calibration purpose with the addition of bandwidth detection circuits. Moreover, the extensive use of digital ΔΣMs for reconfiguration promises small active area and low power consumption if migrated to a deep sub-micron technology.

6.3.1. Proposed Architecture of a Reconfigurable Filter

6.3.1.1. Overview

Figure 48 shows a block diagram of a reconfigurable G_m-C filter. The filter consists of an anti-aliasing filter (AAF), two G_m-C biquads, two passive one-pole LPFs, and a digital controller including six ΔΣMs. Each G_m-C biquad produces a second-order transfer function. Therefore, two G_m-C biquads can make up to fourth-order transfer function. Various frequency responses such as Butterworth, Chebyshev type-I and II, and Elliptic type can be obtained from the transfer function of G_m-C biquad by reconfiguring each transconductance. The second biquad can be bypassed if second-order response is enough. The AAF is a second order, Butterworth-type LPF with a 30-MHz bandwidth to prevent the aliasing of interferers by the high-frequency noise generated from the following ΔΣMs.

Simple passive LPFs consisting of a resistor and a capacitor are placed at the output of each biquad to further reject the high-frequency noise from ΔΣMs.

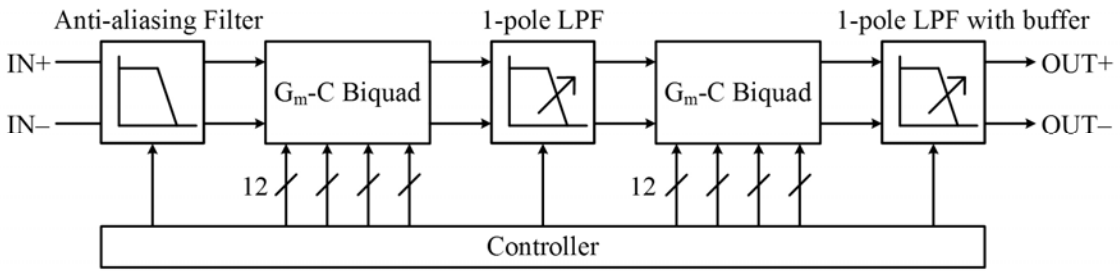


Figure 48. Block diagram of the reconfigurable G_m-C filter.

Figure 49 shows the configuration of G_m-C biquad. It consists of four G_m cells, two op-amps, and six capacitors. The transfer function of this biquad is shown in (28). To generalize the transfer function and get the relationship between each parameter, a general second-order transfer function is introduced in (29) and compared with (28), giving the relationship of (30). For the simple implementation, all capacitor values are fixed, and only G_m is controlled. Therefore, for the given natural frequency, ω_0, and quality factor, Q, each G_m value can be calculated from the equations shown in (30). For the Butterworth and Chebyshev type-I responses, there shouldn't be a zero in their transfer function, so k_2 is set to zero by making *en_cx* as zero. For the Chebyshev type-II and Elliptic configuration, *en_cx* is set to one.

$$\frac{V_o}{V_i} = \frac{s^2 \frac{C_X}{C_B} + \frac{g_{m1}g_{m2}}{C_A C_B}}{s^2 + s\frac{g_{m3}}{C_B} + \frac{g_{m2}g_{m4}}{C_A C_B}} \tag{28}$$

$$\frac{V_o}{V_i} = \frac{k_2 s^2 + k_0}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{29}$$

$$\begin{aligned} C_X &= k_2 C_B \\ g_{m1} &= k_0 C_A / \omega_0 \\ g_{m2} &= \omega_o C_B \\ g_{m3} &= \omega_o C_B / Q \\ g_{m4} &= \omega_o C_A \end{aligned} \tag{30}$$

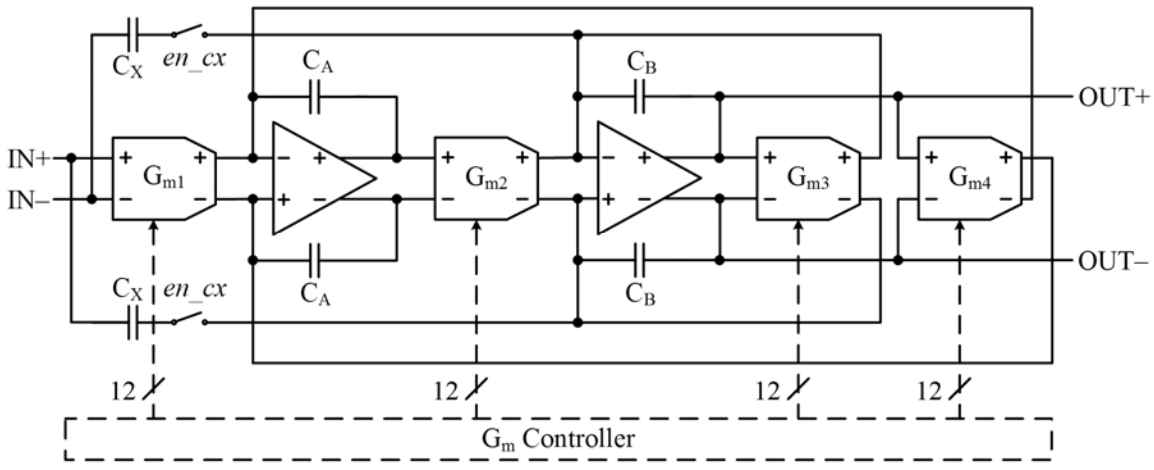


Figure 49. Block diagram of G_m-C biquad.

6.3.1.2. Reconfigurable G_m cell

Figure 50 describes the reconfigurable G_m cell. It consists of a parallel connection of 38 unit cells, where three unit G_m cells are for the negative integer generation, 28 unit G_m cells are for the positive integer generation, and seven unit G_m cells are for the fractional number generation. All the unit G_m cells are identical, as shown in Figure 51.

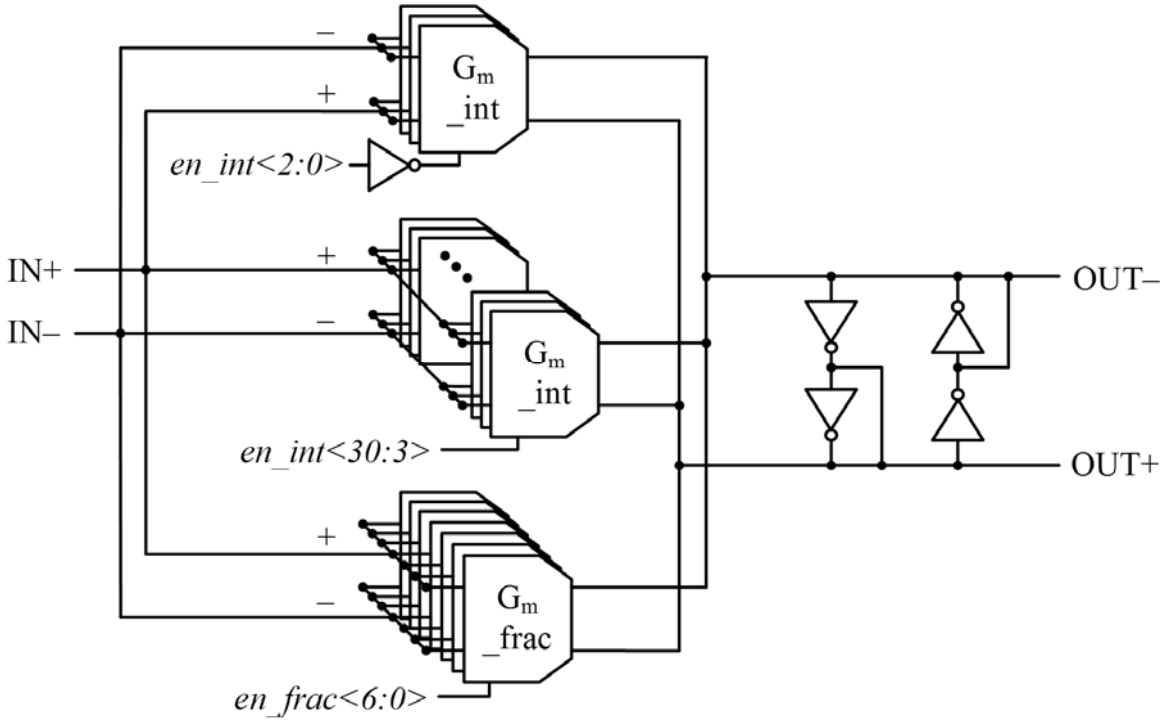


Figure 50. Reconfigurable G_m cell.

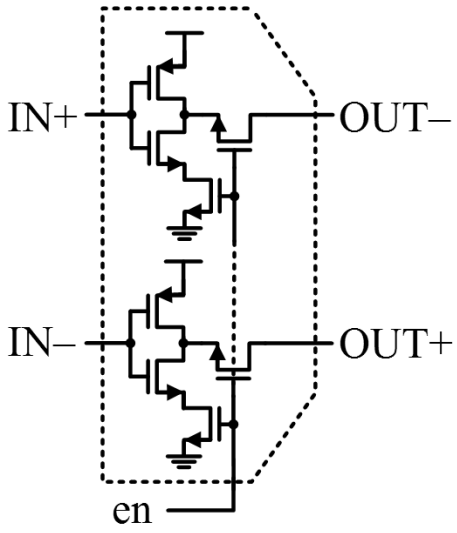


Figure 51. Unit G_m cell using inverters.

The total transconductance is determined by the enabled number of parallel unit G_m cells. The unit G_m cell is based on inverters for simple implementation and good linearity. The output common-mode voltage is self-biased using additional four inverters between the output nodes [32].

Transconductance control is split into five-bit integer part and seven-bit fractional part, as shown in Figure 52. Because the fractional control signals, *en_frac<6:0>*, produce a fractional number from three to four, the integer control signals, *en_int<30:0>*, are configured to produce from –3 to 28, making the overall effective multiplication factor to be a fractional number between 0 and 32. Once the desirable filter type and bandwidth are decided, the target transconductance of each G_m cell is calculated from the transfer function of (28) and (30). While the integer control signal is fixed for a given configuration, the fractional control signals from ΔΣMs are changed at the clock frequency of 300 MHz. The high-speed dithering of ΔΣ modulation moves the quantization noise to a higher frequency so that the in-band noise can be reduced, and the fine fractional resolution is achieved.

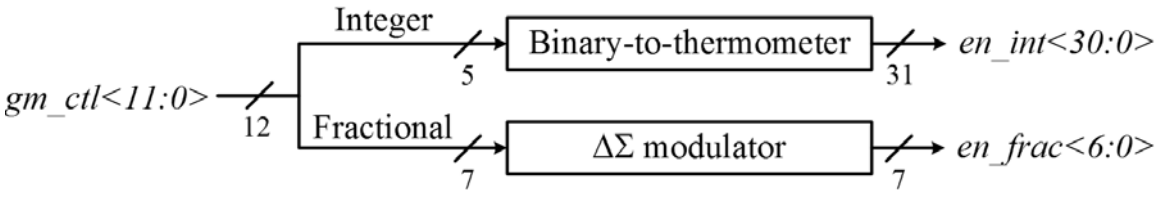


Figure 52. Control scheme of reconfigurable G_m cell.

6.3.1.3. Binary-to-thermometer Code Converter

Because the reconfigurable G_m cell consists of the unit G_m cells, the binary input control signals for the integer part should be converted to the thermometer code. As shown in Figure 52, the integer control signal consists of five bit binary code. To convert this five bit binary code to 32 bit thermometer code, a binary-to-thermometer code converter is designed, as shown in Figure 53, performing two-step conversion: row and column decoding followed by local decoding [33]. Five bit binary code is divided into the upper three bits and the lower two bits for the row decoder and the column decoder, respectively.

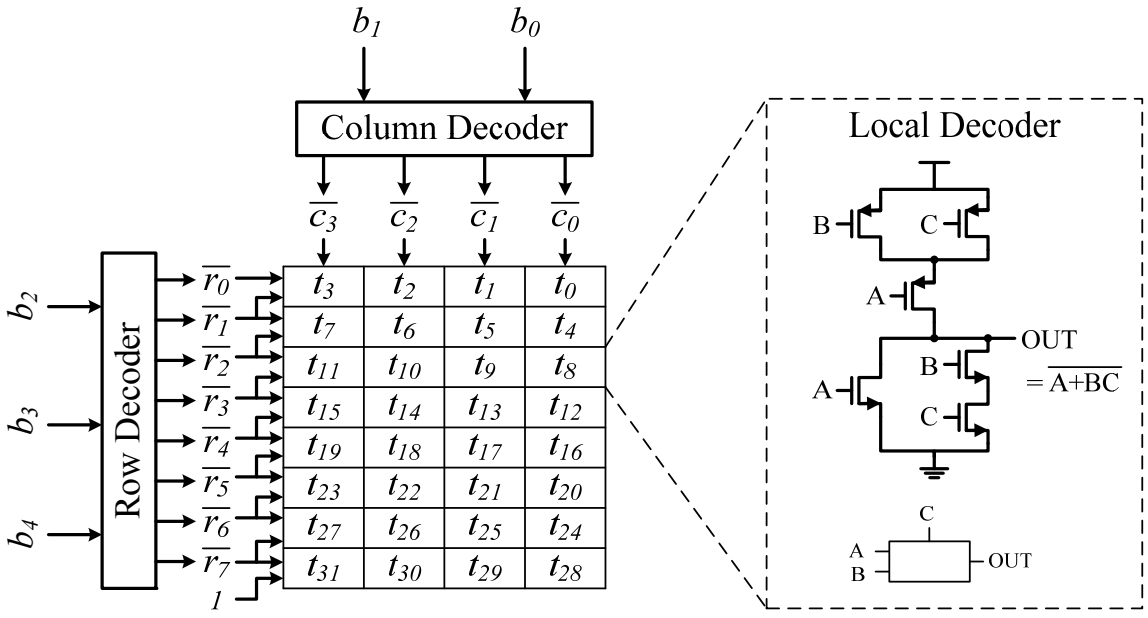


Figure 53. Matrix floor plan for five bit binary-to-thermometer code converter and local decoder.

The row decoder is three bit binary-to-thermometer code converter, as shown in Table 7. The logical equations for the actual implementation are shown in (31). The column decoder is two bit binary-to-thermometer code converter, as shown in Table 8. The logical

equations for the actual implementation are shown in (32). The outputs of the row and column decoders are combined in the local decoder to generate the final 32 bit thermometer code.

Table 7. Three bit binary-to-thermometer code conversion for row decoder.

Binary			Thermometer							
b_2	b_1	b_0	t_7	t_6	t_5	t_4	t_3	t_2	t_1	t_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1
1	0	1	0	0	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1

$$\begin{aligned} &\overline{t_7} = \overline{b_2 b_1 b_0},\ \overline{t_6} = \overline{b_2 b_1},\ \overline{t_5} = \overline{b_2\left(b_1 + b_0\right)},\ \overline{t_4} = \overline{b_2}, \\ &\overline{t_3} = \overline{b_2 + b_1 b_0},\ \overline{t_2} = \overline{b_2 + b_1},\ \overline{t_1} = \overline{b_2 + b_1 + b_0},\ \overline{t_0} = 0 \end{aligned} \tag{31}$$

Table 8. Two bit binary-to-thermometer code conversion for column decoder.

Binary		Thermometer			
b_1	b_0	t_3	t_2	t_1	t_0
0	0	0	0	0	1
0	1	0	0	1	1
1	0	0	1	1	1
1	1	1	1	1	1

$$\overline{t_3} = \overline{b_1 b_0},\ \overline{t_2} = \overline{b_1},\ \overline{t_1} = \overline{b_1 + b_0},\ \overline{t_0} = 0 \tag{32}$$

6.3.1.4. ΔΣ Modulator for Fractional G_m Control

Figure 54 illustrates the architecture of the third-order multi-stage noise shaping (MASH)-type ΔΣM for fractional G_m control [31]. The ΔΣM consists of three digital accumulators, registers and inverters. In the digital accumulator, the delayed carry-out signal is fed back to carry-in of the seven-bit adder, so that the minimum sequence lengths can be increased, resulting in the improved noise shaping property [34]. Each signal of seven-bit output stream toggles the unit G_m cell with the clock frequency of 300 MHz for the fractional transconductance generation. The transfer function of this ΔΣM is shown in (33).

$$\begin{aligned} en\_frac &= C_1 z^{-2} + C_2 z^{-1}\left(1 - z^{-1}\right) + C_3\left(1 - z^{-1}\right)^2 \\ &= \frac{z^{-3}}{1 - z^{-1}/2^7}\left[gm\_ctl\right] + \frac{\left(1 - z^{-1}\right)^3}{1 - z^{-1}/2^7}\left[\text{noise}\right] \end{aligned} \tag{33}$$

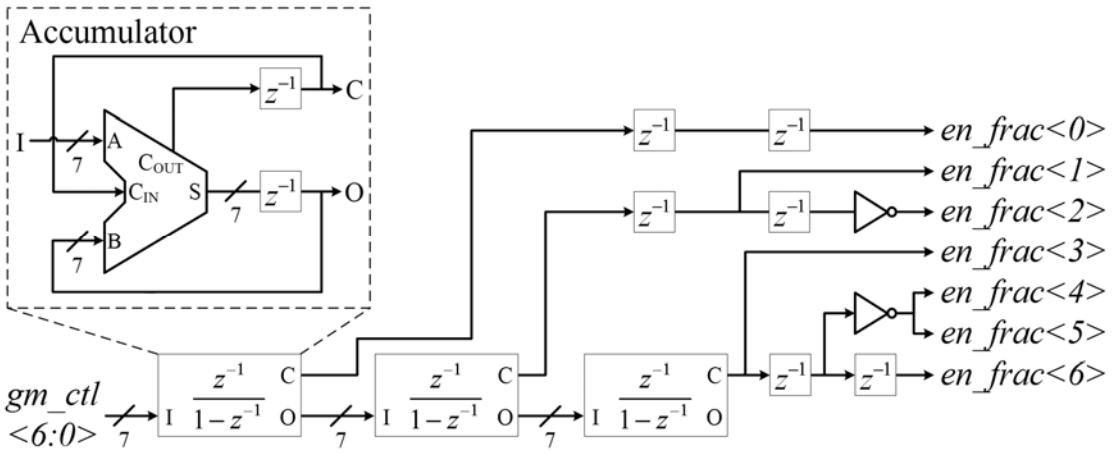


Figure 54. Third-order MASH ΔΣM for fractional G_m control.

By cascading three first-order ΔΣMs and combine their output with proper timing, third-order noise shaping property can be achieved. The output of this ΔΣM is a delayed version of the input signal with the quantization noise shaped by third-order high-pass filtering effect, as shown in (33). The simulated power spectral density with DC input is shown in Figure 55. With the increased minimum sequence length, negligible spurs are observed at the output of the ΔΣM.

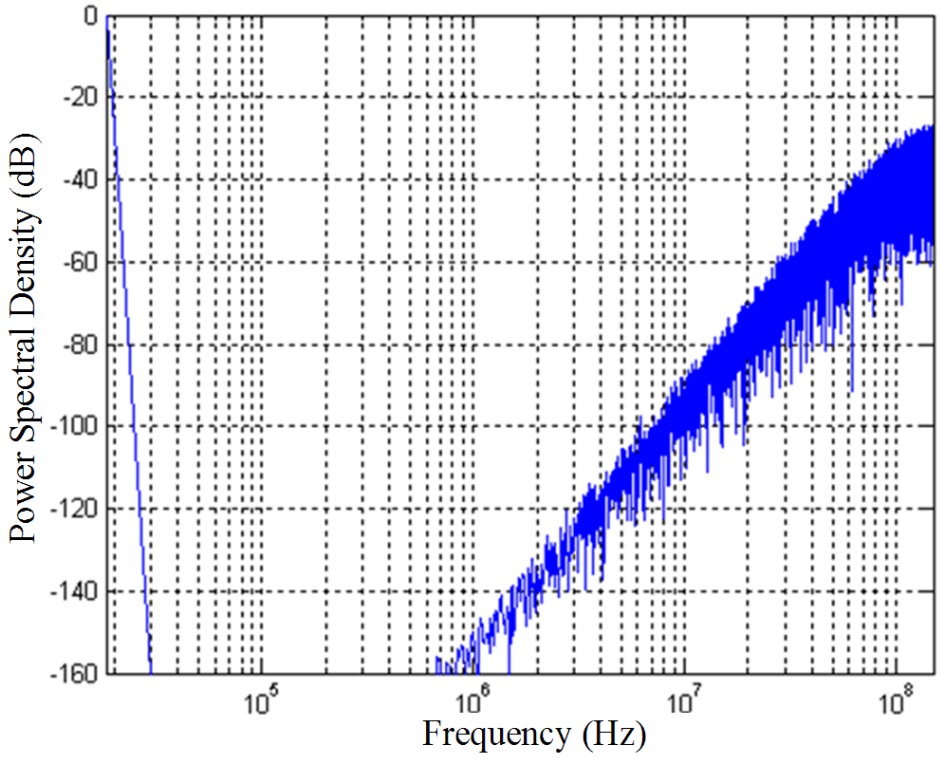


Figure 55. Power spectral density plot at the output of third-order MASH ΔΣM.

As an example, the control values for the 3-dB bandwidth of 10 MHz on each filter type are shown in Table 9 after one-point calibration is performed to compensate for the process, supply voltage and temperature variations. The adjustment of bandwidth control is done by

scaling *gm_ctl* in proportion to the bandwidth change between the test signal and the measured 3-dB bandwidth. Each number in Table 9 means the effective number of unit G_m cells required for each transconductor. To minimize the power consumption of ΔΣMs, G_{m2} and G_{m4} are chosen to have the same value. Moreover, when the transconductance of one G_m cell is the same as others, the output of the ΔΣM can be shared so the unused ΔΣMs can be turned off. Those sharing of the ΔΣMs are represented in Table 9 as the ΔΣ number put in brackets. For example, Butterworth type can share ΔΣ#1 for control of G_{m1}, G_{m2}, and G_{m4} of the first biquad as well as G_{m1}, G_{m2}, and G_{m4} of the second biquad. Therefore, eight G_m cells can be controlled by six and less number of ΔΣMs.

Table 9. Transconductance control value examples for the 10 MHz cut-off frequency.

Control / Type	*en_cx*	*gm_ctl* for the first biquad			*gm_ctl* for the second biquad		
		G_{m1}	$G_{m2,m4}$	G_{m3}	G_{m1}	$G_{m2,m4}$	G_{m3}
Butterworth	0	8.336 (ΣΔ#1)	8.335 (ΣΔ#1)	6.377 (ΣΔ#3)	8.336 (ΣΔ#1)	8.335 (ΣΔ#1)	15.401 (ΣΔ#6)
Chebyshev-I	0	4.406 (ΣΔ#1)	8.279 (ΣΔ#2)	2.326 (ΣΔ#3)	8.279 (ΣΔ#2)	4.406 (ΣΔ#1)	5.616 (ΣΔ#6)
Chebyshev-II	1	3.586 (ΣΔ#1)	8.388 (ΣΔ#2)	6.177 (ΣΔ#3)	20.249 (ΣΔ#4)	8.657 (ΣΔ#5)	15.888 (ΣΔ#6)
Elliptic	1	1.957 (ΣΔ#1)	8.296 (ΣΔ#2)	2.144 (ΣΔ#3)	19.446 (ΣΔ#4)	4.585 (ΣΔ#5)	5.760 (ΣΔ#6)

The actual control bits for G_{m1} of the Butterworth case are presented in Figure 56. From Table 9, the desirable transconductance of G_{m1} is calculated as 8.336 times larger than the transconductance of the unit G_m cell. The desired transconductance multiplication factor of

8.336 is represented to 12 bit number, *gm_ctl*<11:0>, consisting of five bit integer and seven bit fractional numbers, as shown in Figure 52. The integer part is transformed to the thermometer code, *en_int*<30:0>. Because *en_int*<2:0> is inverted before being connected to the enable pin of the unit G_m cell, integer eight will turn on only five positive unit G_m cells. The rest is generated by fractional control. In other words, the average of *en_frac*<6:0> will be 3.336 in this case.

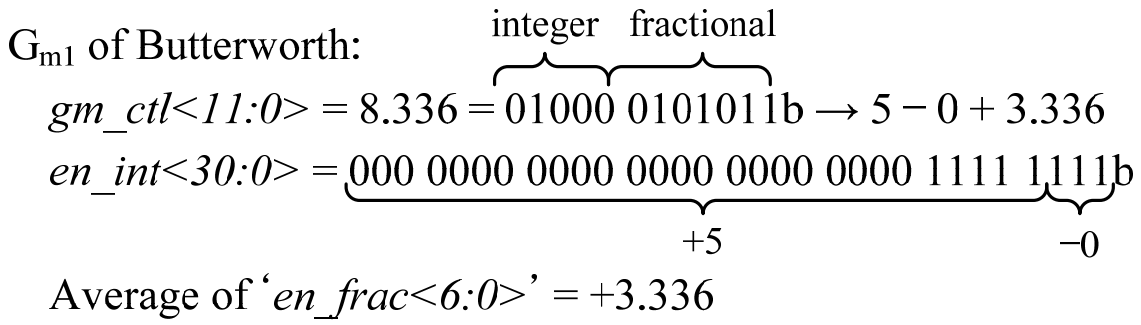


Figure 56. Control value examples for G_{m1} of Butterworth type.

6.3.2. Simulation Results

The reconfigurable baseband G_m-C filter using ΣΔ modulation is designed in a 0.18μm CMOS technology. The top-level simulation has been performed to verify the filtering characteristics. Because of the existence of ΣΔMs for the fractional control resolution, the conventional simulation method for a continuous-time filter design cannot be used. Usually, a continuous-time filter is designed with AC simulators, which linearize the circuits around the DC operating point and calculate the transfer function of the circuit assuming that all the circuits are linear. However, time-varing ΣΔM's output prevents the use of AC simulators. Therefore, AC simulators are used only for the coarse bandwidth

verification, and fine fractional bandwidth control is verified by performing the transient simulation and doing the FFT of the output of the filter to get the frequency response of the filter.

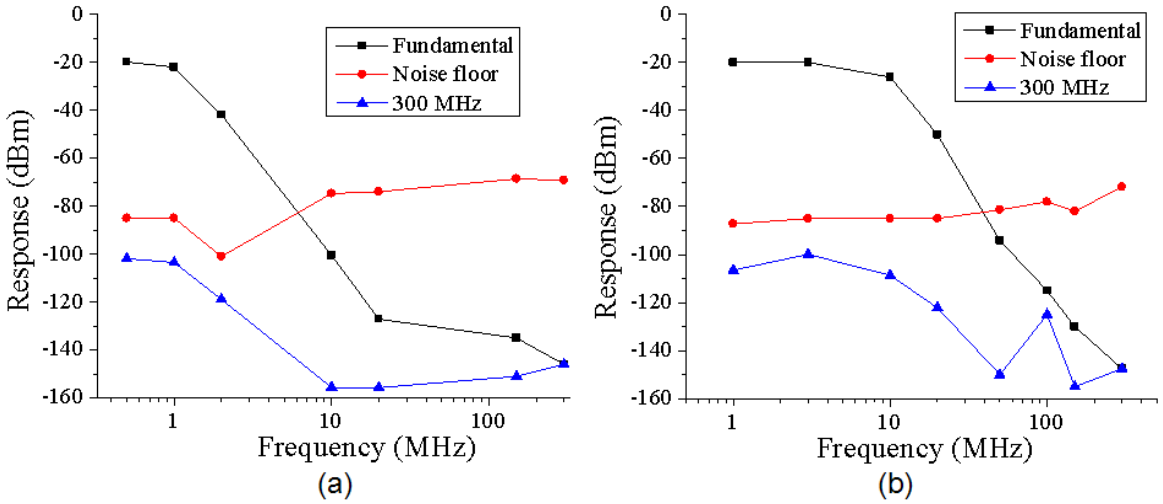


Figure 57. Simulation results of fourth-order Butterworth response with the bandwidth of (a) 1 MHz and (b) 10 MHz.

Figure 57 shows the simulation results for fourth-order Butterworth configuration with the bandwidth of 1 MHz and 10 MHz, respectively. Each simulation has been performed by doing transient simulation with various input frequencies with the amplitude of 200 mV_{pp} and taking the FFT of the filter output. On each FFT result, the amplitude of the input signal, noise floor, and the ΣΔM clock frequency component have been extracted. The fundamental signal shows the filtering effect by the fourth-order filter with the desirable 3-dB frequency bandwidth. Moreover, by adequate filtering, ΣΔM noise has been verified to be sufficiently suppressed, simulated to be always below the noise floor.

6.3.3. Measurement Results

Figure 58 shows the fabricated die micrograph. The die size is 1.7 mm × 1.0 mm including pads. To prevent the digital switching noise from corrupting analog blocks, additional guard ring is drawn with separate power lines between analog blocks and ΔΣMs.

To test the fabricated IC, the chip is mounted and wire-bonded to the custom-designed test board and connected to the CR testbed system, as shown in Figure 59. The input signal is generated by the arbitrary function generator with the differential output. The output of the filter is measured with the spectrum analyzer. Control of equipments and the IC is performed through the custom-designed MATLAB™ program via Ethernet connection or the serial bus interface.

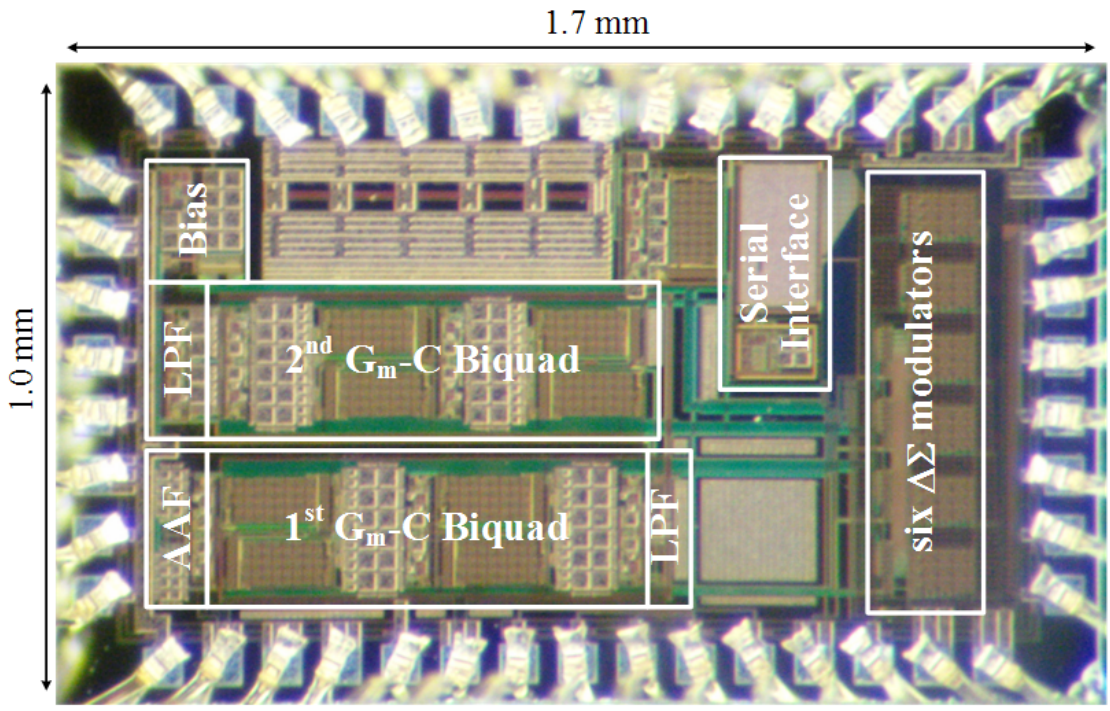


Figure 58. Die micrograph of the reconfigurable analog baseband filter.

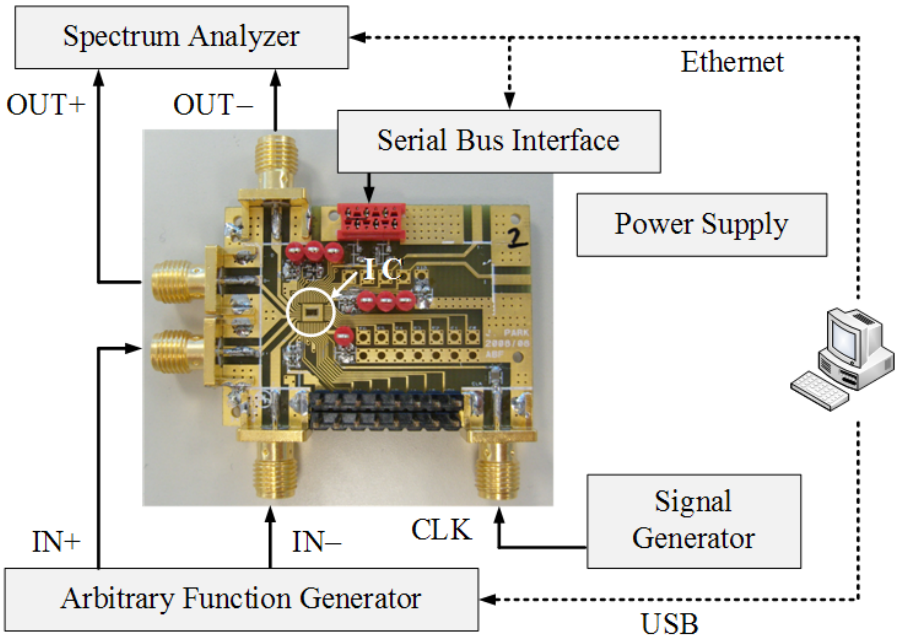


Figure 59. Test environment using CR testbed.

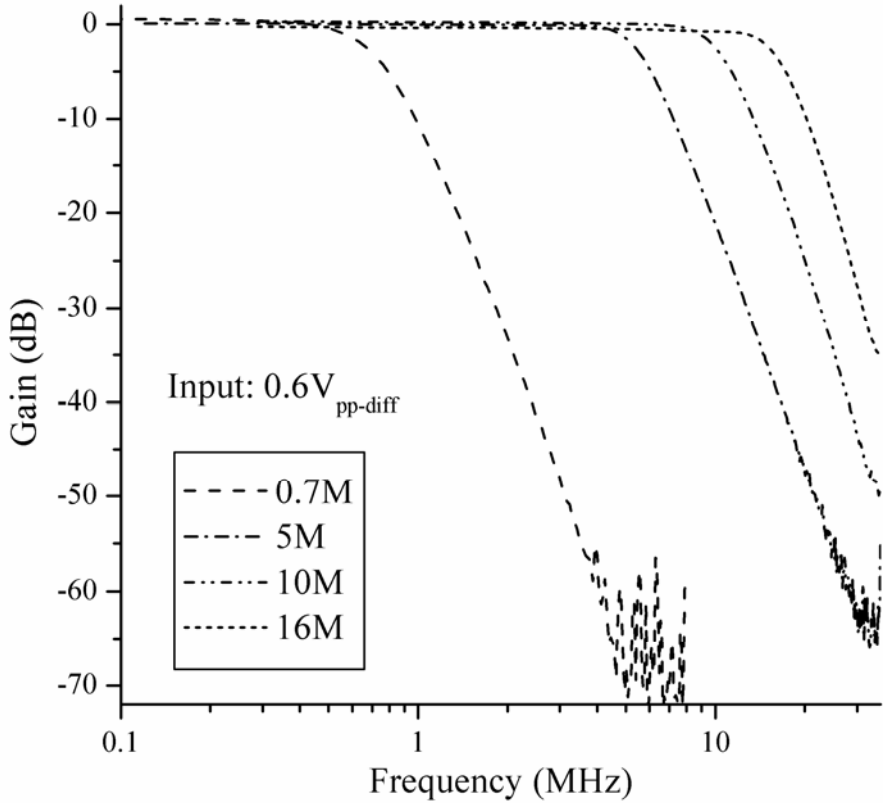


Figure 60. Measured fourth-order Butterworth type frequency response with bandwidth reconfiguration from 0.7 MHz to 16 MHz.

Figure 60 shows the measurement results of the fourth-order Butterworth configuration with the 3 dB cut-off bandwidth varying from 700 kHz to 16 MHz by adjusting the transconductance with digital control. The input signal is chosen to be 0.6 $V_{pp\text{-}diff}$. The dynamic range of the filter is measured to be about 55 dB. Fine bandwidth tuning of 30 kHz step around 10 MHz is also shown in Figure 61, indicating 0.3% tuning resolution which is better than conventional approaches.

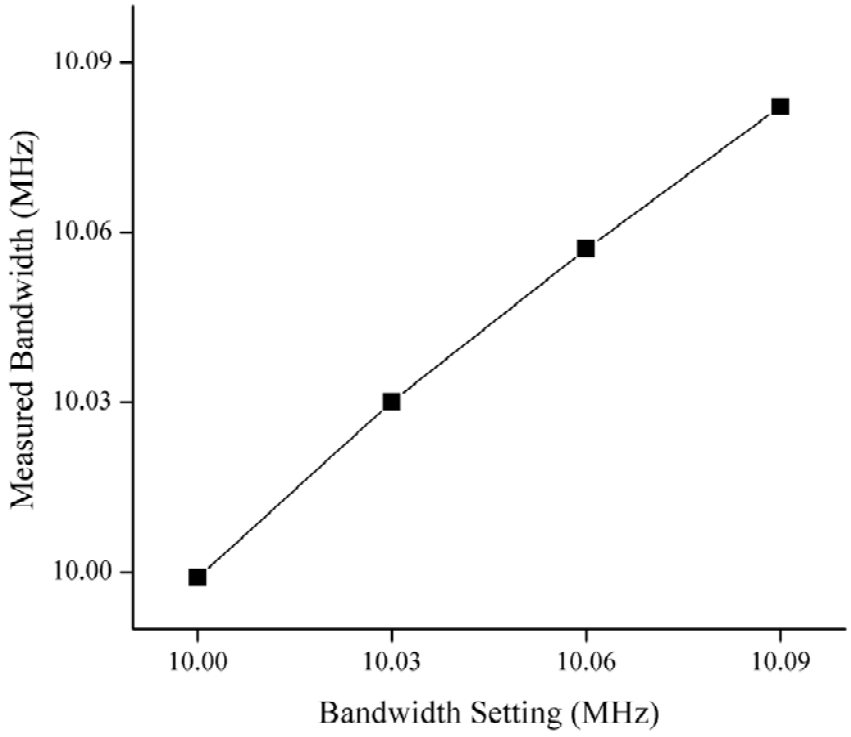


Figure 61. Measured fourth-order Butterworth type fine 3-dB bandwidth tuning around 10 MHz with 30 kHz step.

Figure 62 shows the measured frequency response of various filter types such as Butterworth, Chebyshev type-I and II, and Elliptic with the settings, as shown in Table 9. Butterworth and Chebyshev type-II configuration have a flat pass-band response, while

Chebyshev type-I and Elliptic configuration have a ripple in the pass band. Among four possible configurations, Elliptic has the sharpest transition from the pass band to the stop band. The in-band input 1dB gain-compression point (P_{1dB}) is measured to be 1.8 $V_{pp\text{-}diff}$ with the power supply voltage of 1.6 V, as shown in Figure 63.

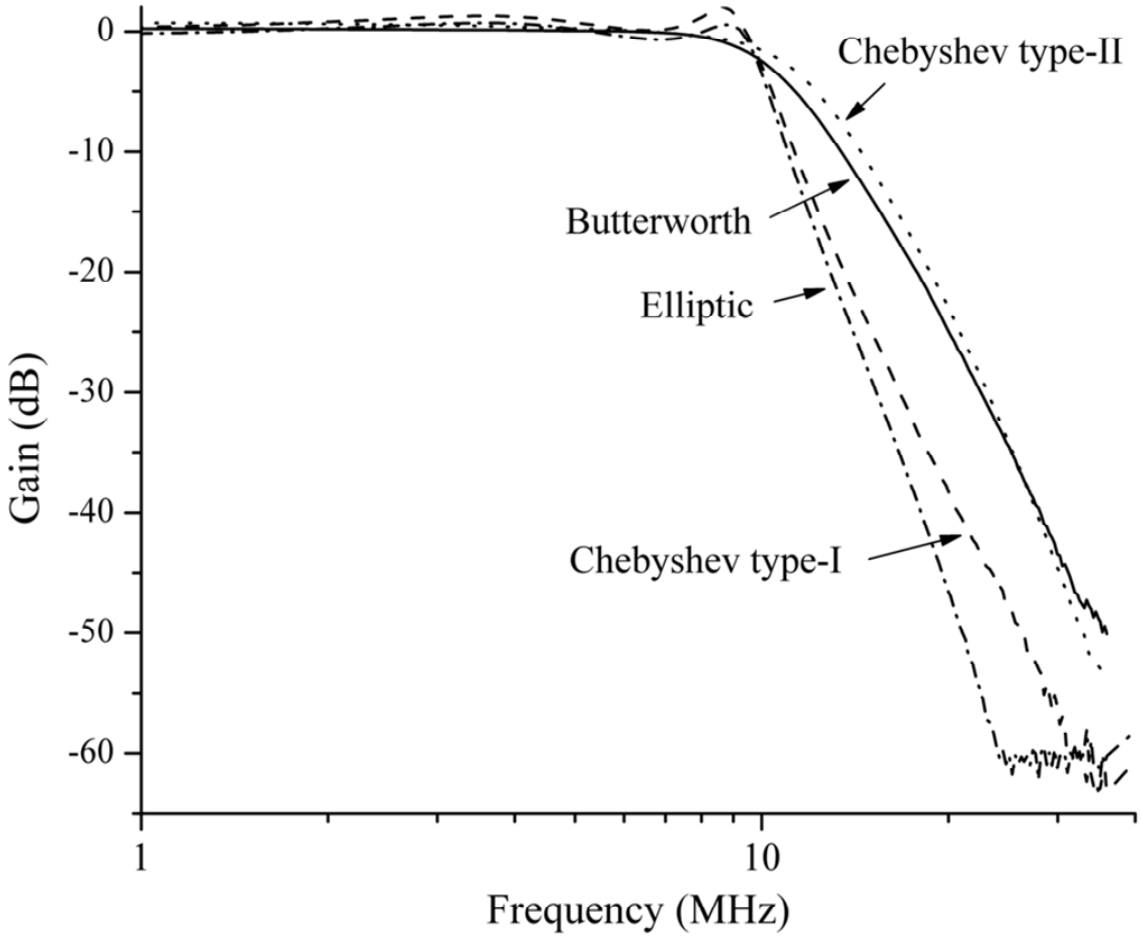


Figure 62. Measured frequency response of various filter types with the 10 MHz bandwidth.

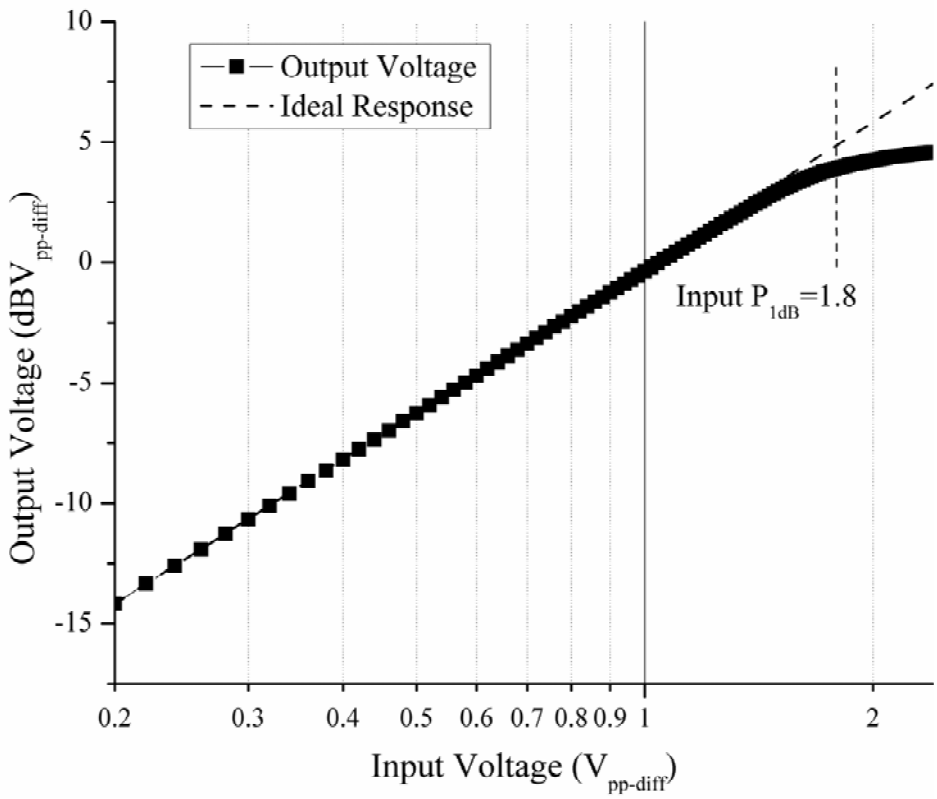


Figure 63. In-band input P_{1dB} measurements with fourth-order 10 MHz bandwidth Butterworth type configuration.

6.3.4. Summary

The reconfigurable baseband G_m-C filter using ΔΣ modulation is fabricated in a 0.18 μm CMOS technology. The active die area is 0.73 mm^2, as shown in the die micrograph of Figure 58. The filter consumes from 19.2 mW to 26.1 mW from a 1.6V supply for the fourth-order filtering depending on the filter type. One ΔΣM consumes about 2.3 mW, so the power difference is mainly due to the turning off the unnecessary ΔΣMs for Butterworth and Chebyshev type-I responses. The digital ΔΣMs and the inverter-based G_m

cells become more beneficial when migrated into the low-supply voltage deep sub-micron technology. Moreover, its high reconfigurability of the filter type and the bandwidth with fine resolution makes it suitable for CR applications. Table 10 summarizes the performance of the proposed filter. Compared with the conventional designs, it has higher bandwidth control resolution than others because of the use of ΔΣMs for fractional transconductance control.

Table 10. Performance summary of the proposed filter and comparisons.

	This work	[28]	[29]	[30]
Topology	G_m-C	Active-G_m-RC	G_m-C	G_m-C
Technology	CMOS 0.18μm	CMOS 0.13μm	CMOS 0.25μm	CMOS 90nm
Area	0.73mm^2	1.56mm^2*	0.15mm^2	0.57mm^2
Power Consumption	19.2~26.1mW	0.72~21.6mW	70mW	5mW
Filter Type	2nd & 4th order Butterworth Chebyshev (I, II) Elliptic	2nd, 4th, 6th order Butterworth	4th order Butterworth	4th order Butterworth Chebyshev Elliptic
f_{-3dB} Tuning Range	0.7~16MHz	0.35~23.5MHz	60~350MHz	0.4~12MHz
Tuning Resolution @ $f_{-3dB,max}$	0.3%	1.3%	N.A.	3.13%

* Area Including VGA

CHAPTER 7

CONCLUSION AND FUTURE WORKS

7.1. Technical Contributions and Impact of the Dissertation

The objective of the research in this dissertation is to develop analog spectrum processing techniques for cognitive radio (CR) applications in CMOS technology.

CR systems aim to use the unoccupied spectrum segments only when the primary users are not present. Therefore, the successful deployment of CR systems relies on their ability to accurately sense the spectrum status as fast as possible. Meanwhile, to maximize the utilization of the available spectrum segments, the bandwidth of the signal has to be highly flexible, thereby requiring a tunable baseband filter.

In this research, an analog spectrum sensing method as well as a highly flexible analog baseband filter architecture is established and implemented in 0.18 μm CMOS technology. Both designs are targeting the utilization of the analog signal processing capability with the aid of the digital circuits. The contributions of this research are as follows:

1. A reconfigurable CR testbed system is established as groundwork for the researches related with CR systems. With this testbed system, the CR system concept and the interference analysis are demonstrated.
2. As the proposed spectrum sensing techniques, analog auto-correlation (AAC) and multi-resolution spectrum sensing (MRSS) are suggested as the feature detection

and energy detection method, respectively. Both methods aim to relax the requirements of an ADC by performing most of computations in the analog domain.

3. A method for determining sensing threshold for MRSS functionality is presented and confirmed with the simulations.
4. A fully integrated MRSS receiver in 0.18 μm CMOS technology is designed and demonstrated. Measurements using the CR testbed system show that the MRSS receiver can works like a simple spectrum analyzer embedded into a receiver. When a 100-kHz $\cos^4$ window is used, detectable sensitivity of -74 dBm with a 32-dB dynamic range was obtained.
5. A reconfigurable CMOS analog baseband filter which can change its bandwidth, type and order with high resolution for CR applications is presented. The proposed filter can be configured as Butterworth, Chebyshev type-I and II, and Elliptic type with the variable bandwidth from 0.7 MHz to 16 MHz.

7.2. Scope of the Future Research

In this dissertation, analog spectrum processing techniques for CR applications are investigated, especially concentrated on spectrum sensing and spectrum filtering techniques.

In the area of spectrum sensing, there is a room for improvement on the performance of the MRSS receiver. Current sensitivity and dynamic range are not enough to meet the spectrum sensing requirement. Moreover, the area and the power consumption should be reduced to become a cost-effective solution. In the area of spectrum filtering, the additional

current consumption from the use of high frequency ΔΣMs should be reduced through further optimization.

Even though spectrum sensing and spectrum filtering techniques are essential functionalities for CR applications, there remains another major challenge; a wide-band transceiver design. Most of the current transceiver designs are optimized for a specific frequency band or communication standard. The major design bottlenecks are on the design of the wide-band LNA and power amplifier (PA). Therefore, the design of a multi-mode, multi-band transceiver has been one of the research topics under active pursuit, and will be the extension of this research.

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